CHAPTER 3

Bipolar Junction Transistors

Learning Objectives

After completing this chapter, you will learn the following:

- Comparison between a bipolar junction transistor and a vacuum triode.
- Basics of transistor construction and types (PNP and NPN transistors).
- Different transistor configurations – common base, common emitter and common collector.
- Transistor input and output characteristics.
- Ebers–Moll model of a transistor.
- Transistor specifications and maximum ratings.
- Different transistor packages and lead identification.
- How to test a transistor.
- Phototransistors and power transistors.

Bipolar junction transistors (BJTs) are three-layer, three-terminal semiconductor devices. They comprise either an N-type semiconductor layer sandwiched between two P-type semiconductor layers or a P-type layer sandwiched between two N-type layers. The former is referred to as a PNP transistor while the latter as an NPN transistor. The first transistor was developed a long time back in the year 1947 by Walter H. Brattain and John Bardeen at the Bell Telephone Laboratories, USA. Before the invention of transistors, vacuum tubes were used extensively. Transistors have replaced the vacuum tubes in most of the applications as they offer considerable advantages over the vacuum tubes, such as smaller size, lighter weight, better efficiency, no warm-up period, lower operating voltages and so on. Transistors form the fundamental building block of the circuitry that governs the operation of computers, cellular phones, power electronics and many other modern electronic systems. In these systems, transistors are used as either amplifiers or electrically controlled switches. In fact, the invention of transistors has revolutionized the field of electronics.

This chapter covers all the fundamental topics related to transistors. We will begin the chapter with a brief comparison of transistors with vacuum triodes, followed by fundamental topics such as transistor construction, types, different transistor configurations and transistor input and output characteristics. Topics of practical interest, such as transistor specifications, maximum ratings, lead identification and transistor testing, are covered towards the end of the chapter.

3.1 Bipolar Junction Transistor versus Vacuum Triode

Both bipolar junction transistors and vacuum triodes are three-terminal devices. Transistors can be considered as solid-state analogs of vacuum triodes. The three terminals of a triode are referred to as cathode, plate and control grid. The corresponding terminals of a transistor are emitter, collector and base, respectively. Although both transistors and vacuum triodes are three-terminal devices, their modes of operation are fundamentally different. Transistors are current-controlled devices whereas vacuum triodes are voltage-controlled devices. In a vacuum triode, the output voltage is directly related to the input voltage. The amplification factor (μ) of a vacuum triode is defined as the ratio of the change in the plate voltage to the change in the grid voltage for a constant plate current. In a transistor the output current is a function of the input current, and the transistor gain (β) is defined as the ratio of the change in the collector current to the change in the base current for a constant collector–emitter voltage.

3.2 Transistor Construction and Types

A BJT is a three-layer, three-terminal semiconductor device having two PN junctions. It comprises three differently doped semiconductor regions, namely the emitter region, the base region and the collector region. The base region is physically sandwiched between the emitter and the collector regions. BJT are so named as both holes and electrons contribute to the flow of current.

The width of the base region is much smaller than the width of the emitter and the collector regions. Typical ratio of the total width of the transistor to the width of the base region is of the order of few hundreds. The emitter region is the most heavily doped, the collector region moderately doped and the base region very lightly doped. The doping of the base region is around 10 times less than that of the emitter region. This results in reduced conductivity of the base region. Bipolar transistors can be classified as NPN and PNP transistors depending upon the type of doping of the three regions.

NPN Transistor

Figure 3.1(a) shows the structure of an NPN transistor. As is evident from the figure, the collector and the emitter regions are N-type semiconductors and the base region is a P-type semiconductor. The collector, emitter and base terminals are designated as C, E and B, respectively. Figure 3.1(b) shows the circuit symbol of an NPN transistor. The arrow on the emitter lead specifies the direction of the conventional current flow when the emitter–base junction is forward-biased. In an NPN transistor most of the current flow is due to flow of electrons.

PNP Transistor

Figure 3.2(a) shows the structure of a PNP transistor. The collector and the emitter regions are P-type semiconductors and the base region is an N-type semiconductor. Figure 3.2(b) shows the circuit symbol of a PNP

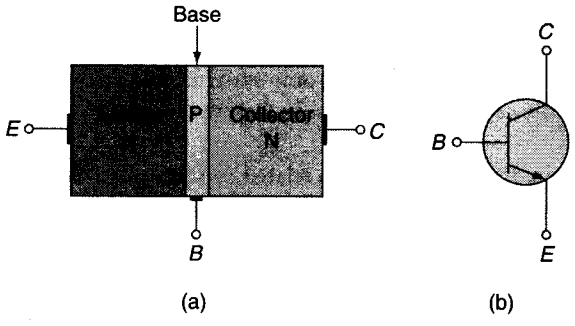


Figure 3.1 | (a) Structure; (b) circuit symbol of an NPN transistor.

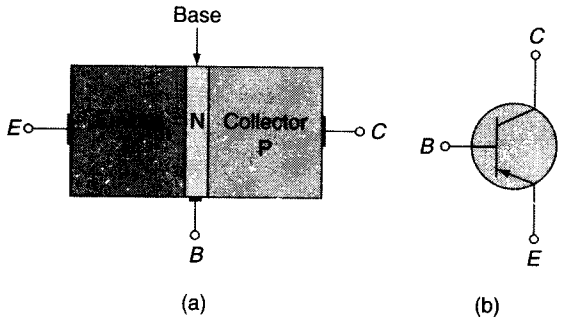


Figure 3.2 | (a) Structure; (b) circuit symbol of a PNP transistor.

transistor. The arrow on the emitter lead specifies the direction of the conventional current flow when the emitter–base junction is forward-biased. In a PNP transistor, holes contribute mostly to the flow of current.

NPN transistors are more commonly used as compared to PNP transistors as they offer higher current density and faster switching times. This is so because the electron mobility is higher than the hole mobility.

3.3 Transistor Operation

The basic operation of an NPN transistor is described in this section. The operation of a PNP transistor is same as that of an NPN transistor except that the roles of electrons and holes are interchanged and the polarities of the voltages and the direction of current reversed. Transistors may be looked upon as two PN junction diodes connected back to back. The two junctions are the emitter–base junction and the collector–base junction. The fundamentals of semiconductor junction diodes covered in Chapter 2 apply to transistors also and will be used to explain the operation of a transistor. As we have studied in Chapter 2, when the PN junction diode is an open circuit no current flows through it and the diode voltage is equal to the diode's contact potential. Similarly, when no external voltage is applied to the transistor, the currents flowing through the transistor are zero and the potential at the two junctions is equal to their respective contact potentials.

Transistors operate in four regions, namely the active region, the reverse-active region, the saturation region and the cut-off region depending upon the polarity of voltages applied to the emitter–base and the collector–base junctions. In the active region, the emitter–base junction is forward-biased and the collector–base junction is reverse-biased. Transistors when operating in the active region function as amplifiers. In the reverse-active region, the biasing condition is reversed, that is, the emitter–base junction is reverse-biased and the collector–base junction is forward-biased. Transistors are seldom operated in the reverse-active region. In the saturation region, both the emitter–base and the collector–base junctions are forward-biased and in the cut-off region both the junctions are reverse-biased. When the transistor is used as a switching device, it operates either in the saturation or the cut-off region. It acts as a closed switch in the saturation region and as an open switch in the cut-off region. When used as an amplifier, the transistor is operated in the active region.

Let us consider the operation of an NPN transistor in the active region. As mentioned before, in the active region the emitter–base junction is forward-biased and the collector–base junction is reverse-biased. When the emitter–base junction is forward-biased with an open collector–base junction [Figure 3.3(a)], normal PN junction diode action takes place. The width of the depletion region decreases due to the applied bias and there is a heavy flow of electrons from the N-type emitter to the P-type base. As the base is lightly doped,

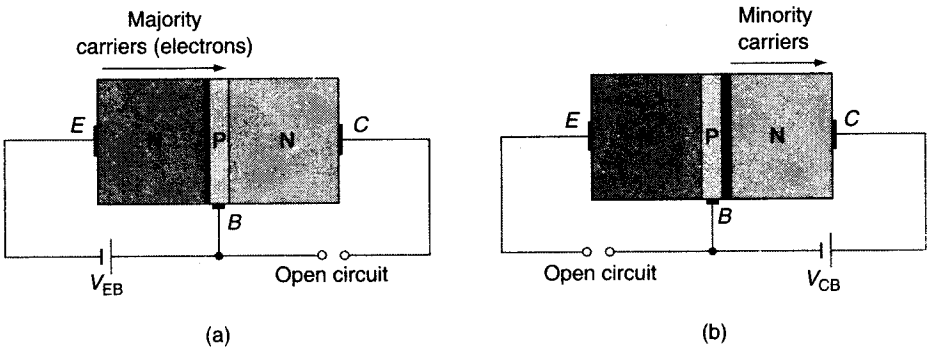


Figure 3.3 | (a) Forward-biased emitter–base junction; (b) reverse-biased collector–base junction.

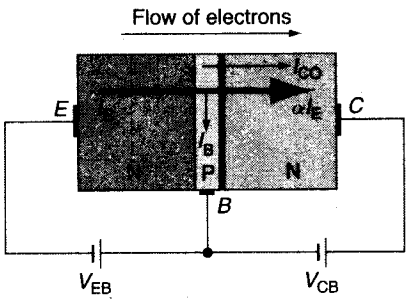


Figure 3.4 | Flow of current in an NPN transistor in the active region.

a very small hole current flows from the P-type base to the N-type emitter region. The width of the depletion region is larger in the base region as compared to that in the emitter region as the base is lightly doped compared to the emitter region. If the collector–base junction is reverse-biased with the emitter–base junction open [Figure 3.3(b)], it behaves like a normal reverse-biased junction diode. There is a small current flow due to the minority carriers, that is, the flow of electrons from the base region to the emitter region and flow of holes from the emitter to the base. The depletion width increases with the increase in the reverse-bias voltage and is larger in the base region than that in the collector region.

Figure 3.4 shows the flow of current in an NPN transistor in the active region, that is, both the forward and the reverse voltages are applied simultaneously to the emitter–base and the collector–base junctions, respectively. The emitter current (I_E) comprises electron current (due to flow of electrons from emitter to base) and hole current (due to the flow of holes from base to emitter). As the base is very lightly doped as compared to the emitter, the emitter current consists mainly of electrons. Not all the electrons crossing the emitter–base junction reach the collector–base junction as some of them remain in the base region and constitute the base current (I_B). As the base region is very thin and has low level of conductivity (as it is lightly doped), only a very few electrons remain in the base region. The rest of the electrons diffuse into the reverse-biased collector–base junction. They travel across the collector–base junction easily as they are minority carriers in the P-type base region of the collector–base junction. This is referred to as the injection of the minority carriers into the P-type

base region. (It may be recalled that in a reverse-biased PN junction diode, the minority carriers easily cross the junction). These electrons diffuse across the reverse-biased junction to reach the N-type collector and constitute the collector current (I_C). The magnitude of the base current is of the order of few microamperes as compared to several milliamperes for the collector and the emitter current.

Applying Kirchhoff's current law to the transistor, considering it as a node, we get

$$I_E = I_C + I_B \tag{3.1}$$

where I_E is the emitter current, I_C the collector current and I_B the base current.

From Eq. (3.1) we can infer that the emitter current is the sum of the collector current and the base current. The collector current comprises two components: the majority-carrier component and the leakage-current component. The majority-carrier component is due to the electrons that have traveled from the emitter region across the base to the collector region. This component is equal to αI_E, where α is the fraction of emitter electrons that reach the collector region. The leakage current (I_{CO}) is the minority current of the reverse-biased collector–base junction with an open-circuit emitter–base junction. I_{CO} is in the range of few hundreds of nanoamperes to few microamperes. The expression for collector current is given by

$$I_C = \alpha I_E + I_{CO} \tag{3.2}$$

The above equation is only valid in the active region of the transistor. The generalized expression for the collector current in a transistor is given by

$$I_C = \alpha I_E + I_{CO}\left[1 - \exp\left(-\frac{V_{CB}}{V_T}\right)\right] \tag{3.3}$$

where V_{CB} is the voltage across the collector–base junction and V_T the volt equivalent of temperature.

When the collector–base junction is sufficiently reverse-biased, the term $\exp(-V_{CB}/V_T)$ tends to zero and Eq. (3.3) reduces to Eq. (3.2).

3.4 Common-Base Configuration

Transistors are connected in any of the following three configurations:

1. Common-base (CB) configuration.
2. Common-emitter (CE) configuration.
3. Common-collector (CC) configuration.

CB configuration is discussed in this section. CE and the CC configurations are covered in Sections 3.5 and 3.6, respectively.

In the CB configuration, the base terminal is common to both the input and the output sections. Figures 3.5(a) and (b) show the basic circuit of the transistor in the CB configuration for the NPN and the PNP transistors, respectively. The directions of currents shown are used for conventional current flow. Also, the current flowing into the transistor is taken as positive and the current leaving the transistor is taken as negative.

Input Characteristics

The input characteristics of a transistor are a plot of the input current versus the input junction voltage for different values of output junction voltage. The input characteristics of CB configuration relate the emitter current (I_E) to the emitter–base voltage (V_{EB}) for various levels of the collector–base voltage (V_{CB}). Figure 3.6 shows the input characteristics of a common-base NPN Silicon transistor. The current

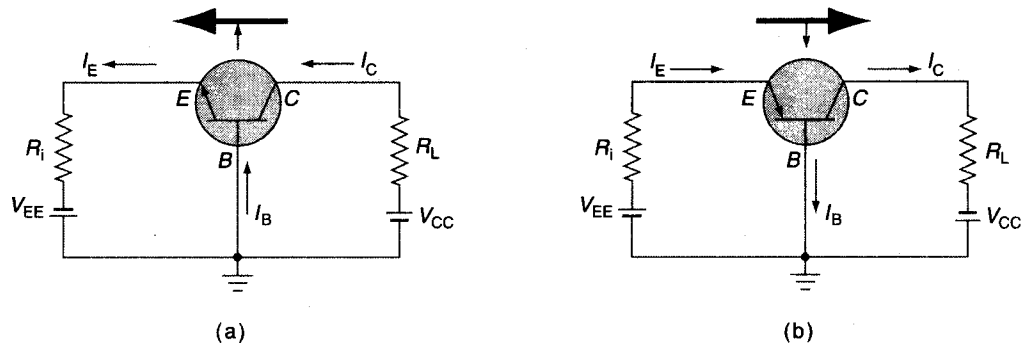


Figure 3.5 | Common-base configuration.

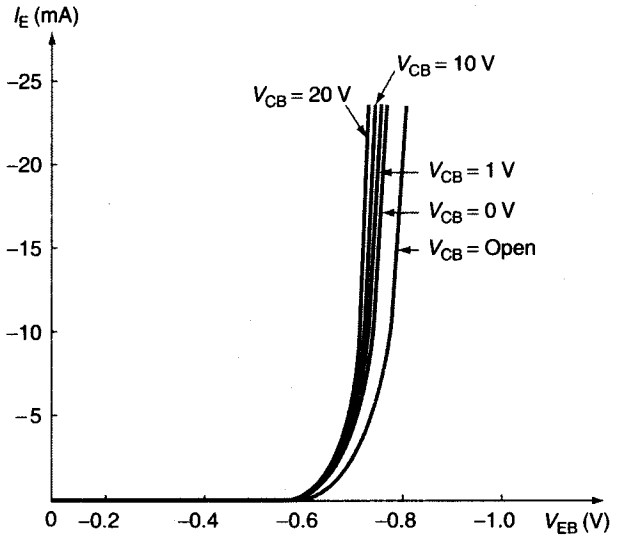


Figure 3.6 | Input characteristics of CB transistor.

I_E is considered negative as the current flows out of the emitter terminal. The input characteristics of PNP transistors are same with the reversal of polarity of the voltages and direction of currents.

From the figure we can infer that there is a cut-in or threshold voltage below which the value of emitter current is very small. The typical values of cut-in voltage for silicon and germanium transistors are approximately 0.5 and 0.1 V, respectively. The curve for open condition is the same as that for a forward-biased PN junction diode. Another feature of the input characteristics is that for a fixed value of collector-base voltage (V_{CB}), the emitter-base voltage (V_{EB}) increases with increase in the emitter current (I_E). This behavior is the same as that of a PN junction diode in the forward-biased state. Since a small change in the emitter-base voltage causes a very large change in the emitter current, the input resistance (r_i) of the common-base configuration is very small. The value of r_i in the linear portion of the input characteristics is of the order of hundred ohms. Also it can be interpreted from the figure that for fixed value of emitter-base voltage (V_{EB}), the emitter current (I_E) increases with increase in the collector-base voltage (V_{CB}). This is because of the early effect phenomenon in transistors.

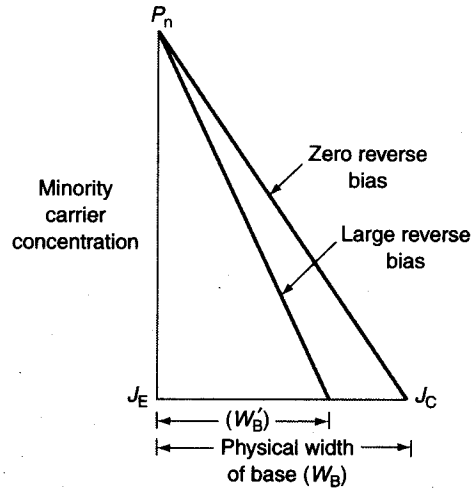


Figure 3.7 | Early effect.

Early effect or the *base width modulation* phenomenon refers to the change in the width of the base region with the change in the collector–base voltage. As the emitter–base junction is forward-biased, the width of the depletion region is negligible. For the reverse-biased collector–base junction, the width of the depletion region is substantial. The width of the depletion region increases with increase in the reverse voltage at the collector–base junction. As the base region is lightly doped, the penetration of the depletion region is much larger in the base region than in the collector region. As a result of this the effective width of the base region decreases. This phenomenon of change in the effective width of the base region with change in the collector–base voltage is referred to as the early effect.

As a result of the early effect, at increased reverse potential the rate of recombination of the electrons and holes decreases. This results in increase in the value of α. Also, the concentration of the minority carriers becomes zero at effective base width (W_B') instead of W_B (Figure 3.7). Hence, the concentration gradient of minority carriers (P_n) is increased within the base region. As the emitter current is proportional to the gradient of minority carriers at the emitter junction (J_E), the value of emitter current also increases.

Output Characteristics

The output characteristics of a transistor are a plot of the output current and the output junction voltage for different values of input current. The output characteristics of common-base configuration (Figure 3.8) relate the collector current (I_C) to the collector–base voltage (V_{CB}) for various levels of the emitter current (I_E). For a fixed value of emitter current, the collector current almost remains constant with changes in the value of the collector–base voltage. However, near the origin the collector current drops rapidly with the decrease in the value of the collector–base voltage. The output characteristics can be divided into three regions, namely the active region, the cut-off region and the saturation region.

Active Region

In the active region the collector–base junction is reverse-biased while the emitter–base junction is forward-biased. The unshaded portion of Figure 3.8 corresponds to the active region. The collector current (I_C) is almost independent of the collector–base voltage (V_{CB}) and depends only on the value of the emitter current (I_E). Therefore, the output characteristics curves are straight parallel lines. Actually the collector

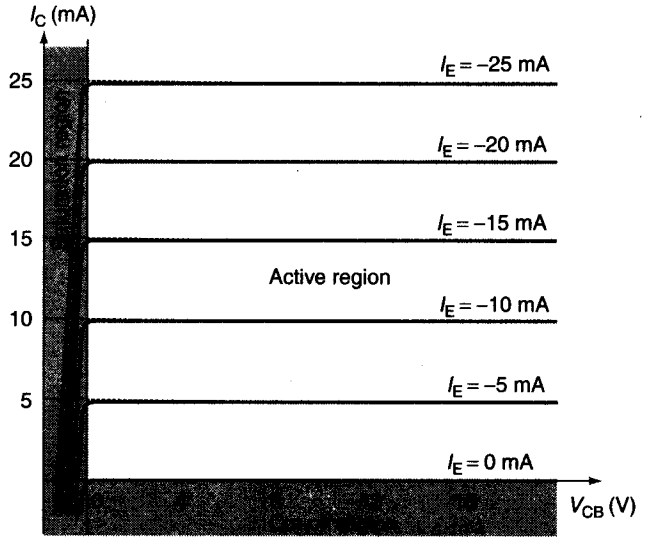


Figure 3.8 | Output characteristics of the common-base transistor.

current increases slowly with the collector–base voltage (around 0.5%). This is because of the early effect phenomenon. But for most applications this increase can be ignored and the collector current can be considered to be constant for a fixed value of emitter current. The output resistance (r_o) offered by the CB configuration is very high as a very large change in the collector–base voltage produces a very small change in the collector current.

When the emitter–base junction is open-circuited, the emitter current is zero. The collector current that flows in this condition is the reverse saturation current (I_{CO}). This condition corresponds to the lowest curve in the output characteristics. The current I_{CO} is of the order of few microamperes for germanium transistors and several nanoamperes for silicon transistors.

Cut-off Region

In the cut-off region, both the collector–base and the emitter–base junctions of a transistor are reverse-biased. The region below the $I_E = 0$ curve corresponds to the cut-off region. In this region, the transistor acts as an open circuit and does not conduct any current. As mentioned before, the value of collector current at $I_E = 0$ is equal to the reverse saturation current (I_{CO}).

I_{CO} increases rapidly with increase in temperature. As an example, for a general purpose silicon transistor 2N2222, the values of I_{CO} at a collector–base voltage of 50 V for ambient temperatures 25°C and 150°C are 10 nA and 10 μA, respectively. This implies that there is a change of the order of 1000 times for 125°C change in temperature. I_{CO} is also referred to as I_{CBO}, the collector current with base open-circuited. I_{CBO} can be ignored in most transistor applications except for power transistors and transistors operating at high temperatures.

Saturation Region

In the saturation region, both the collector–base and the emitter–base junctions are forward-biased. The region to the left of $V_{CB} = 0$ line corresponds to the saturation region. As is clear from the figure, the collector–base voltage (V_{CB}) is slightly negative in the saturation region. This is because the collector–base junction is also

forward-biased. There is an exponential increase in the collector current with a small increase in the collector–base voltage.

Alpha (α)

Alpha (α) is the fraction of emitter current that contributes to the collector current. The current equation in a transistor is given by

$$I_C = I_{CO} + \alpha I_E \tag{3.4}$$

The above equation can be rewritten as

$$\alpha = \frac{I_C - I_{CO}}{I_E - 0} \tag{3.5}$$

Alpha (α) can be defined as the ratio of the increment in the value of collector current from its value in the cut-off region to the increment in the value of emitter current from its value in the cut-off region. As mentioned earlier, the value of I_{CO} is very small and can be ignored in the large-signal analysis. Therefore Eq. (3.4) reduces to

$$I_C = \alpha I_E \tag{3.6}$$

Therefore, α is also referred to as the large-signal current gain for a common-base transistor. In the active region, the value of α is nearly equal to 1, the exact value being between 0.90 and 0.998. Therefore, the current gain of the transistor in the CB mode is less than unity. The value of α is not constant but varies with the emitter current (I_E), collector voltage (V_{CB}) and the operating temperature. The voltage gain of the CB configuration is in the range of 50–300. Therefore, a CB transistor acts as a voltage amplifier and not as a current amplifier.

When a time-varying input is applied, the point of operation moves on the output characteristics curve. In that case an ac alpha (α_{ac}) is defined as the ratio of the change in the collector current to the change in the emitter current for a fixed value of collector–base voltage. Mathematically,

$$\alpha_{ac} = \left(\frac{\Delta I_C}{\Delta I_E}\right)_{V_{CB}=\text{constant}} \tag{3.7}$$

where α_{ac} refers to common-base, short circuit amplification factor.

EXAMPLE 3.1 *For the common-base configuration shown in Figure 3.9, determine the values of base current (I_B), emitter current (I_E) and collector current (I_C). It is given that the value of α is 0.95.*

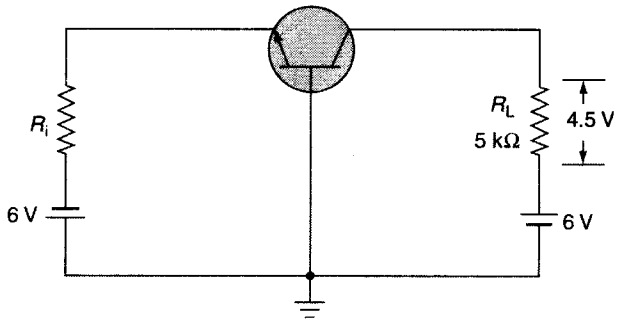


Figure 3.9 | Example 3.1.

Solution

1. The value of load resistance $R_L = 5\ k\Omega$.
2. The voltage drop across the resistor is 4.5 V.
3. Therefore, the current flowing through the resistor = $4.5/(5 \times 10^3)$ A = 0.9 mA.
4. The current flowing through the resistor is the collector current. Therefore, collector current is equal to 0.9 mA.
5. The emitter current is $I_C/\alpha = 0.9 \times 10^{-3}/0.95$ A = 0.947 mA.
6. The base current is $I_E - I_C = (0.947 \times 10^{-3} - 0.9 \times 10^{-3}) = 47\ \mu A$.

Answer: The value of I_C, I_E and I_B are 0.9 mA, 0.947 mA and 47 μA, respectively.

3.5 Common-Emitter Configuration

The common-emitter (CE) configuration has emitter terminal common to both the input and the output sections, as shown in Figures 3.10(a) and (b), for the NPN and the PNP transistors, respectively. The input signal is applied to the emitter–base section and the output is taken from the collector–emitter section. It is the most commonly used transistor configuration. Salient features of CE transistor configuration are high values of voltage and current gains, medium values of input and output impedances.

Input Characteristics

The input characteristics of the transistor in the common-emitter configuration relate the base current (I_B) to the emitter–base voltage (V_{BE}) for different values of the collector–emitter voltage (V_{CE}). The input characteristics for a common-emitter NPN transistor are shown in Figure 3.11. We can see from the figure that the magnitude of base current (I_B) is in range of several tens of microamperes. For fixed value of emitter–base voltage (V_{BE}), an increase in the value of collector–emitter voltage (V_{CE}) results in a decrease in the value of the base current (I_B). This is because of the early effect which results in reduction of the base width with increase in the collector–emitter voltage (V_{CE}).

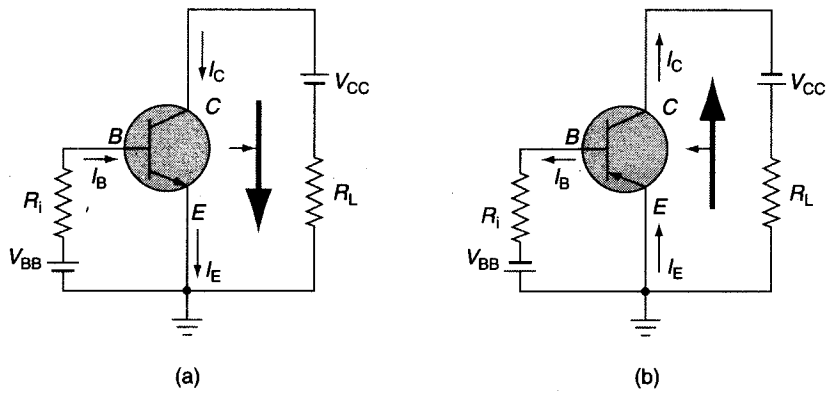


Figure 3.10 | Common-emitter configuration for (a) NPN transistor; (b) PNP transistor.

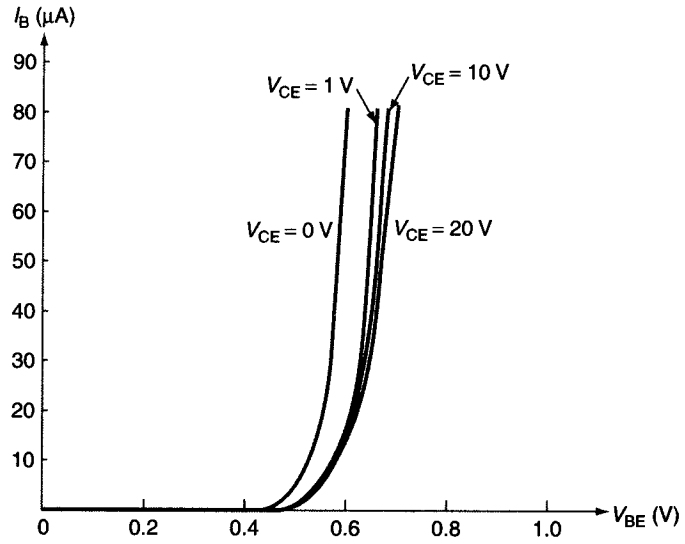


Figure 3.11 | Input characteristics of CE transistor.

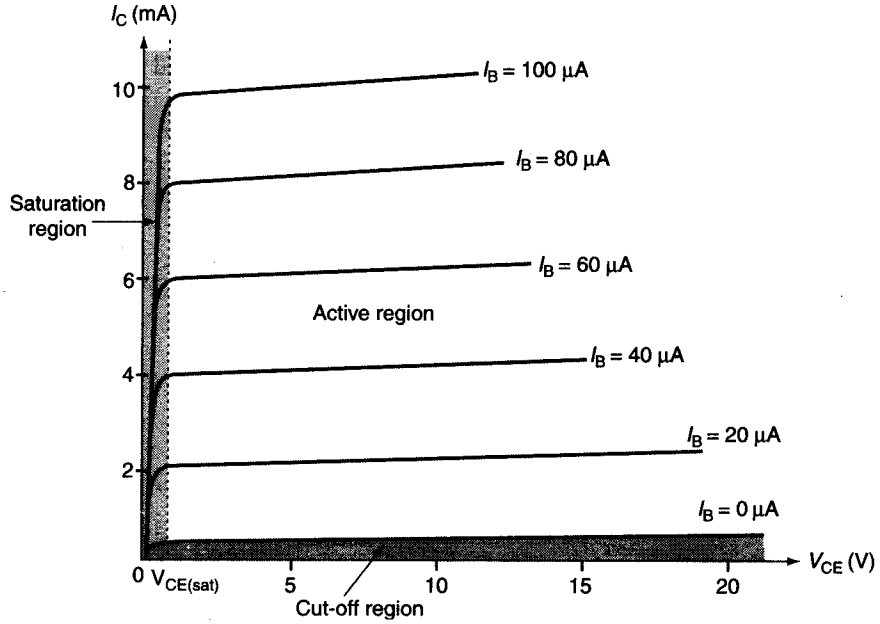


Figure 3.12 | Output characteristics of CE transistor.

Output Characteristics

Output characteristics of the CE configuration relate the collector current (I_C) to the collector–emitter voltage (V_{CE}) for different values of base current (I_B). The output characteristics of a CE transistor are shown in Figure 3.12. The output curves for CE configuration are not as horizontal as that for CB configuration, indicating that the collector–emitter voltage has an influence on the value of collector current.

Beta (β)

For any transistor the emitter, collector and base currents are related to each other by the equation

$$I_E = I_C + I_B \tag{3.8}$$

Relationship between collector and emitter current is also given by

$$I_C = I_{CO} + \alpha I_E \tag{3.9}$$

Combining Eqs. (3.8) and (3.9) we get

$$I_C = \frac{\alpha}{(1-\alpha)} I_B + \frac{1}{(1-\alpha)} I_{CO} \tag{3.10}$$

If we substitute $\beta = \alpha/(1-\alpha)$ then Eq. (3.10) becomes

$$I_C = \beta I_B + (\beta+1) I_{CO} \tag{3.11}$$

Here, β (also denoted as h_{FE}) is referred to as the DC forward current transfer ratio or the DC current gain of the transistor. A very small change in the value of α is reflected as a very large change in the value of β. The CE characteristics of the transistors of the same type number differ significantly from one device to another. The value of β varies considerably with changes in both the operating temperature and collector current (Figure 3.13).

Active Region

As in the case of CB transistor configuration, for CE transistor configuration also the emitter–base junction is forward-biased in the active region and the collector–base junction is reverse-biased. The active region in the output characteristics (Figure 3.12) corresponds to the portion of the graph to the right of the line at $V_{CE(sat)}$ and above the curve for $I_B = 0$. As can be seen from the figure, the curves of collector current (I_C) for different values of base current (I_B) are not as horizontal and parallel as the curves for the CB configuration. Transistors in the CE configuration operating in the active region are used as voltage, current and power amplifiers.
As $I_B >> I_{CO}$ in the active region, therefore, in the active region

$$I_C = \beta I_B$$

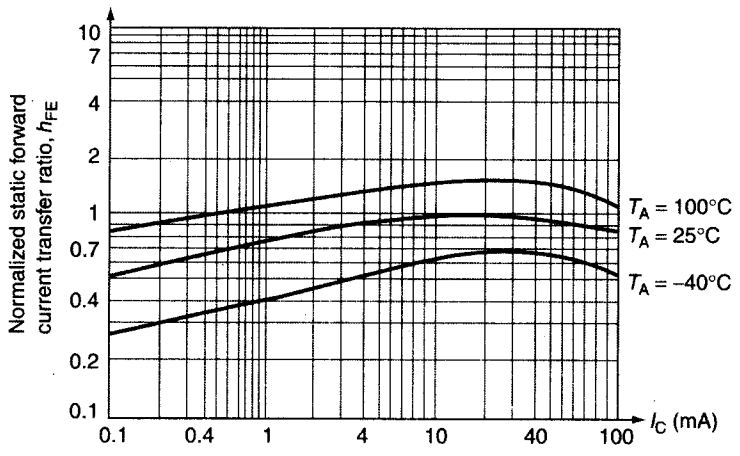


Figure 3.13 | Variation of h_{FE} with change in temperature and collector cur-

Typical value of β is in the range of 50–100. Hence, the CE configuration provides a high current gain. It also provides a large value of voltage and power gain.

For AC applications ac beta (β_{ac}) is defined as

$$\beta_{ac} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}=\text{constant}}$$

β_{ac} is referred to as the CE forward-current amplification factor and is also denoted by h_{fe}.

Saturation Region

The CE transistor is in the saturation region when both the collector–base and the emitter–base junctions are forward-biased. Magnitudes of collector–base voltage (V_{CB}) and emitter–base voltage (V_{EB}) are equal to the cut-in voltages of the collector–base and the emitter–base junctions, respectively. Therefore, the value of V_{CE} ($V_{CB} + V_{BE}$) is few tenths of volts in the saturation region. The region to the left of $V_{CE} = V_{CE(sat)}$ line in the output characteristics is the saturation region. In the saturation region, the value of the collector current is independent of the base current and depends on the value of resistor connected between the collector terminal and the supply terminal. For the CE circuit of Figure 3.10, the value of collector current in the saturation region is given by V_{CC}/R_L. The minimum base current required to saturate the transistor is given by I_C/β.

The parameter which is important in the saturation region is the CE saturation resistance ($R_{CE(sat)}$), which is defined as the ratio of the collector–emitter voltage at saturation to the collector current ($V_{CE(sat)}/I_C$). The curves to the left of the $V_{CE} = V_{CE(sat)}$ line can be approximated as straight lines whose slope can be determined using the value of $R_{CE(sat)}$.

Cut-off Region

In the cut-off region, both the collector–base and the emitter–base junctions are reverse-biased. Also, the base current is equal to zero ($I_B = 0$) in this region. In the CE configuration, for $I_B = 0$, there is a considerable amount of collector current flowing through the transistor. Its value is given by substituting the value $I_B = 0$ in Eq. (3.11):

$$I_C = (\beta + 1)I_{CO} = \frac{I_{CO}}{1-\alpha} \tag{3.12}$$

This current is denoted by the symbol I_{CEO}.

For silicon transistors, the value of α near cut-off region is nearly zero. Therefore, the value of collector current is equal to I_{CO}. Hence, the silicon transistor is in the cut-off region when $I_B = 0$ both for short circuit ($V_{BE} = 0$) and reverse-biased emitter–base junction.

For germanium transistors, the value of α near cut-off region may be as large as 0.9. Therefore, the value of the collector current flowing through the transistor can be as large as 10 times the value of leakage current I_{CO}. Hence, the germanium transistor is not in the cut-off region for $I_B = 0$. A reverse bias needs to be applied to the emitter–base junction to bring the transistor to cut-off. The bias voltage applied should bring the value of collector current (I_C) less than or equal to reverse saturation current (I_{CO}). Reverse-bias voltage of 0.1 V is sufficient to reduce the collector current to this value. Therefore, the germanium transistor is in cut-off region when $I_B = 0$ for reverse-biased emitter–base junction with V_{BE} greater than 0.1 V.

EXAMPLE 3.2 *For a transistor, the value of α is specified to be 0.98 at a particular collector–base voltage. The value of α increases by 0.5% when the collector–base voltage is increased. Find the percentage change in the value of β. Comment on the result.*

Solution

1. Original value of $\alpha = 0.98$.
2. Value of $\beta = \alpha/(1 - \alpha) = 0.98/(1 - 0.98) = 49$.
3. New value of $\alpha = 0.98 + 0.5 \times 0.98/100 = 0.985$.
4. Value of β for $\alpha = 0.985$ is $\beta = 0.985/(1 - 0.985) = 66$.
5. Percentage change in $\beta = [(66 - 49)/49] \times 100\% = 34.69\%$.
6. From the above result it is clear that a small change in the value of $\alpha = 0.5\%$ results in a large change in the value of $\beta = 34.69\%$.

Answer: Percentage change in β is 34.69%.

EXAMPLE 3.3

For the circuit shown in Figure 3.14, find the values of emitter current (I_E), collector current (I_C) and base current (I_B) It is given that $\beta = 50$, $V_{BE} = 0.7$ V and $I_{CO} = 0$ μA.

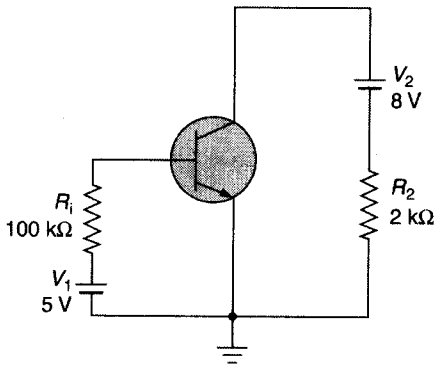


Figure 3.14 | Example 3.3.

Solution

1. The polarity of the voltage V_1 applied to the input section forward biases the emitter–base junction. Therefore the transistor is in active region or in the saturation region. Let us assume that the transistor is in the active region.
2. Applying Kirchhoff's voltage law to the input section:
$$5 - 100 \times 10^3 \times I_B - V_{BE} = 0$$
3. Substituting $V_{BE} = 0.7$ V, $I_B = (5 - 0.7)/(100 \times 10^3) = 43$ μA.
4. $I_C = \alpha I_B$ (as $I_{CO} \cong 0$)
Therefore, $I_C = 50 \times 43 \times 10^{-6}$ A = 2.15 mA.
5. Applying Kirchhoff's voltage law to the output section, we get
$$8 - 2 \times 10^3 \times 2.15 \times 10^{-3} - V_{CE} = 0$$
$$V_{CE} = 8 - 2 \times 10^3 \times 2.15 \times 10^{-3}$$
$$= 8 - 4.3 = 3.7 \text{ V}$$
6. $V_{CE} = V_{CB} + V_{BE}$
Therefore, $V_{CB} = 3.7 - 0.7 = 3$ V.

7. For the NPN transistor, positive value of V_{CB} represents a reverse-biased collector–base junction and hence the assumption that the transistor is in the active region is correct.

8. $I_E = I_C + I_B$. Therefore

$$I_E = 2.15 \times 10^{-3} + 43 \times 10^{-6} = 2.193 \text{ mA}$$

Answer: $I_C = 2.15$ mA, $I_B = 43$ μA and $I_E = 2.193$ mA.

3.6 Common-Collector Configuration

In the common-collector (CC) configuration, also known as the emitter-follower configuration, the collector terminal is common to both the input and the output sections. Figures 3.15(a) and (b) show the NPN and PNP transistors connected in the CC configuration. The configuration is similar to the common-emitter configuration with the output taken from the emitter terminal rather than the collector terminal.

CC configuration offers high input impedance and low output impedance and hence it is used for impedance matching applications, that is, for driving low-impedance load from a high-impedance source. The voltage gain offered by CC configuration is less than unity and the value of current gain is high.

Input Characteristics

The input characteristics of CC configuration relate the base current (I_B) to the collector–base voltage (V_{BC}) for different values of the emitter–collector voltage (V_{EC}). The input characteristics for a CC NPN transistor are shown in Figure 3.16.

Output Characteristics

Output characteristics of the CC configuration relate the emitter current (I_E) to the emitter–collector voltage (V_{EC}) for different values of base current (I_B). Figure 3.17 shows the output characteristics for an NPN transistor in the CC configuration. The characteristics are similar to that for the CE configuration.

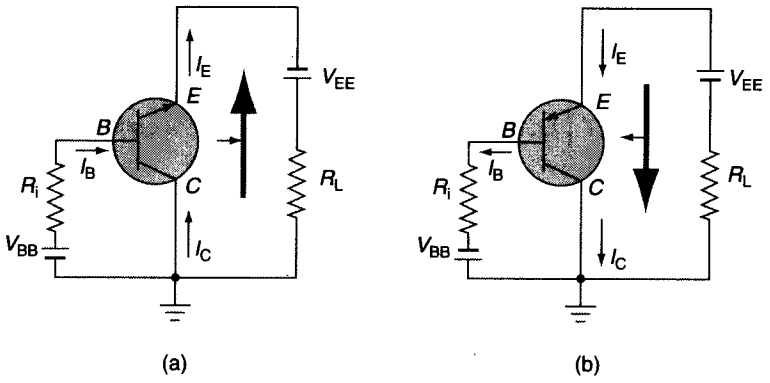


Figure 3.15 | CC configuration for (a) NPN transistor; (b) PNP transistor.

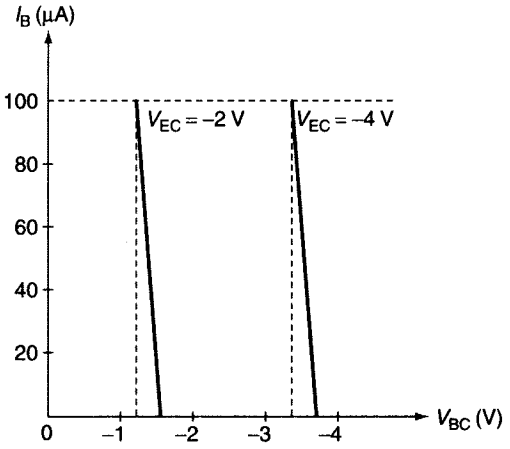


Figure 3.16 | Input characteristics of the CC configuration.

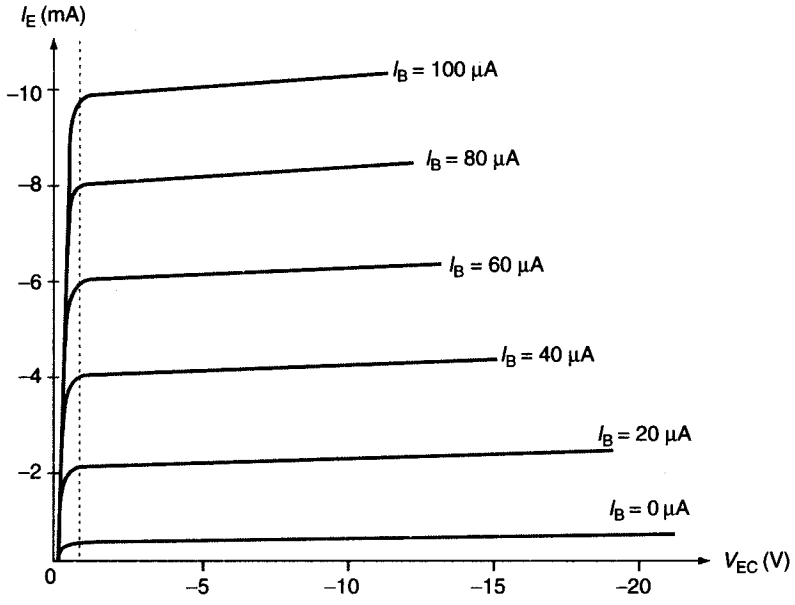


Figure 3.17 | Output characteristics of the CC configuration.

Gamma (γ)

Gamma (γ) is the current gain in the CC configuration. For any transistor the collector–emitter and base currents are related to each other by the expression

$$I_E = I_C + I_B \tag{3.13}$$

Relationship between collector and emitter current is given by

$$I_C = I_{CO} + \alpha I_E \tag{3.14}$$

Combining Eqs. (3.13) and (3.14) we get

$$I_E = \frac{I_B}{1-\alpha} + \frac{I_{CO}}{1-\alpha} \tag{3.15}$$

Table 3.1 | Salient features of the three transistor configurations

Configuration	Current gain	Voltage gain	Input impedance	Output impedance
Common emitter (CE)	High (≈50–100)	Very high (≈500)	Medium (≈800 Ω)	Medium (≈50 kΩ)
Common collector (CC)	High (≈80–100)	Approximately unity	Very high (≈800 kΩ)	Very low (≈50 Ω)
Common base (CB)	Approximately unity	High (≈150)	Low (≈100 Ω)	Very high (≈500 kΩ)

If $\gamma = (\beta + 1) = 1/(1 - \alpha)$ then Eq. (3.15) becomes

$$I_C = \gamma I_B + \gamma I_{CO} \tag{3.16}$$

Table 3.1 gives a qualitative comparison of the three configurations in terms of current and voltage gains, input and output impedances.

The configurations discussed in Sections 3.4–3.6 are the basic ones and only show the mode of operation of the transistor. The associated circuitry to be used in these configurations for providing required biasing to the two junctions will be discussed in detail in Chapter 4.

EXAMPLE 3.4 *Derive an expression for the power gain provided by the transistor in Figure 3.18.*

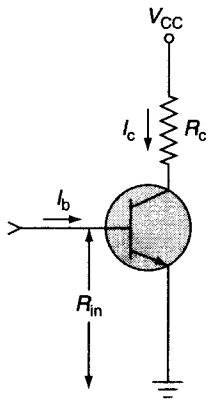


Figure 3.18 | Example 3.4.

Solution

1. Input power = Input voltage × Input current.
2. Input voltage = $I_b \times R_{in}$.
3. Therefore, Input power = $I_b \times R_{in} \times I_b = I_b^2 \times R_{in}$.
4. Output power = Output voltage × Output current
   $= I_c^2 \times R_c$
   $= \beta^2 \times I_b^2 \times R_c$
5. Power gain = Output power/Input power
   $= (\beta^2 \times I_b^2 \times R_c)/(I_b^2 \times R_{in})$
   $= (\beta^2 \times R_c)/R_{in}$

3.7 Ebers–Moll Model of Transistors

Ebers–Moll transistor model was developed by Ebers and Moll in the year 1954. It is also known as the coupled diode model. It is an ideal model for a bipolar transistor and is applicable for all four regions of transistor operation. The model involves two ideal diodes and two ideal current sources. Figures 3.19(a) and (b) show the Ebers–Moll model for the NPN and the PNP transistor, respectively.

To understand the model let us consider the generalized current equation of a transistor given in Eq. (3.3). It is repeated here for convenience of the readers.

$$I_C = I_{CO}\left[1-\exp\left(-\frac{V_{CB}}{V_T}\right)\right] + \alpha I_E \tag{3.17}$$

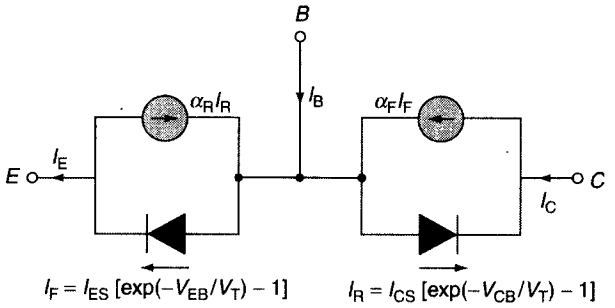
Equation (3.17) can be rewritten for the active region as

$$I_C = I_{CS}\left[1-\exp\left(-\frac{V_{CB}}{V_T}\right)\right] + \alpha_F I_E \tag{3.18}$$

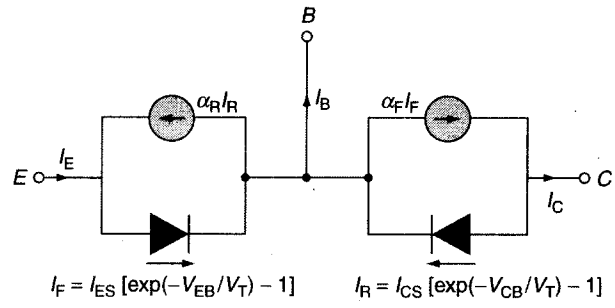
where α_F is the CB current gain in the normal operating mode (emitter–base junction is forward-biased and collector–base junction is reverse-biased) and I_{CS} the saturation current of the collector–base diode.

For the reverse-active region the Eq. (3.17) can be rewritten as

$$I_E = I_{ES}\left[1-\exp\left(-\frac{V_{EB}}{V_T}\right)\right] + \alpha_R I_C \tag{3.19}$$



(a)



(b)

Figure 3.19 | Ebers–Moll model for (a) NPN transistor; (b) PNP transistor.

where α_R is the CB current gain in the inverting operating mode (emitter–base junction is reverse-biased and the collector–base junction is forward-biased) and I_{ES} the saturation current of the emitter–base diode.

The two diodes shown in Figure 3.19 represent the base-emitter and the collector–base diodes and are connected back-to-back. The reverse saturation currents through the emitter–base and the collector–base diodes are I_{ES} and I_{CS}, respectively. Two current sources are in shunt with the diodes and their values depend upon the current flowing through the diodes. They quantify the transport of minority carriers through the base region, that is, they account for the minority-carrier transport across the base.

From Figure 3.19, the equations for the collector, emitter and base currents in the Ebers–Moll model are given by

$$I_C = -I_R + \alpha_F I_F \tag{3.20}$$

$$I_E = I_F - \alpha_R I_R \tag{3.21}$$

$$I_B = (1 - \alpha_R) I_R + (1 - \alpha_F) I_F \tag{3.22}$$

The Ebers–Moll parameters are related by the expression

$$I_{ES}\alpha_F = I_{CS}\alpha_R \tag{3.23}$$

This expression is referred to as the reciprocity relation.

In the discussion above, we have not taken into consideration the base-spreading resistance ($r_{bb'}$) of a transistor. It is the resistance offered by the base region to the flow of current through it. Typical value of $r_{bb'}$ is of the order of 100 Ω and it increases with the increase in the reverse-bias collector–base voltage. Its value also depends on the doping level of the base region. The effects of $r_{bb'}$ are important at high frequencies.

It may be mentioned here that it is impossible to construct a transistor by simply connecting two diodes back-to-back in series. A cascade arrangement of two diodes exhibits transistor properties only if the carriers injected by one junction diffuse into the second junction.

3.8 Transistor Specifications and Maximum Ratings

Selecting the right transistor type number suiting one's requirements becomes a simple exercise provided we can appreciate the critical specifications of a transistor and also their significance for different applications. Some of the important transistor specifications are: DC current gain (β or h_{FE}), AC current gain (β_{ac} or h_{fe}), gain-bandwidth product (f_T), transistor breakdown voltages and maximum power dissipation ($P_{D(max)}$).

DC Current Gain (β or h_{FE})

The variable β (also denoted as h_{FE}) is called the DC current gain, that is, the ratio of the collector current to the base current of the transistor in common-emitter configuration. It specifies the base current required to keep the transistor conducting for a given collector current. It is an important parameter for switching transistors as it tells about the minimum base current required to drive the transistor in the saturation region for a certain collector current. A transistor with smaller h_{FE} needs a harder base drive for a given collector current.

AC Current Gain (β_{ac} or h_{fe})

AC current gain is defined as the ratio of the change in the collector current to a small change in the base current for a constant collector–emitter voltage:

$$h_{fe} = \left(\frac{\Delta I_C}{\Delta I_B} \right)_{V_{CE} = \text{constant}} \tag{3.24}$$

Gain-Bandwidth Product (f_T)

The gain-bandwidth product (f_T) tells us about the high frequency response of the transistor. It is the frequency for which gain on the high-frequency side falls to unity or 0 dB. It is an important parameter that needs to be considered when the transistor is to be used for intermediate frequency/radio frequency (IF/RF) applications.

Transistor Breakdown Voltages

There are two types of breakdown phenomena possible in a transistor, namely the avalanche breakdown and reach-through phenomenon. The breakdown voltages associated with the avalanche multiplication are V_{CEO} and V_{CBO}. V_{CEO} is the maximum voltage that can be applied across the collector–emitter junction with the base open in the CE configuration. It is the worst case of collector–emitter breakdown voltage and is a very important specification particularly in switching transistors used in switched-mode power supplies. This parameter is often specified in different ways. Quite often, V_{CER} (collector–emitter breakdown voltage with a specified resistance typically of the value of 100–200 Ω connected between the base and emitter) and V_{CES} (collector–emitter breakdown voltage with base shorted to the emitter) ratings are also given in addition to the V_{CEO} rating of the switching transistors. It may be mentioned that V_{CEO} is the lowest of all and if the design is such that the V_{CEO} rating is not exceeded, the possibility of collector–emitter junction breakdown gets eliminated. V_{CBO} is the reverse output breakdown voltage when the transistor is connected in the CB configuration with the emitter terminal open.

The second mechanism that leads to transistor breakdown is the reach-through or the punch-through effect. It results from the increase in the width of the collector–base junction depletion region with increase in the reverse voltage. As the base region is very thin, even at moderate values of reverse voltages, the depletion region spreads completely across the base and reaches the emitter junction. This results in large flow of emitter current leading to transistor breakdown. The collector–base breakdown voltage due to the punch-through effect is independent of the transistor configuration.

The lower of the breakdown voltages either due to avalanche or reach-through breakdown is considered as the maximum voltage limit.

$I_{C(max)}$

It is the peak collector current rating of the transistor. It is specified for continuous or pulsed mode of operation of a transistor.

Power Dissipation ($P_{D(max)}$)

It is the maximum power dissipation capability of a transistor. The curve for maximum power dissipation can be plotted using the formula

$$P_{D(max)} = V_{CE} \times I_C \tag{3.25}$$

The maximum collector current, collector–emitter voltage and the power ratings limit the active region of operation of a transistor as shown in Figure 3.20. $V_{CE(sat)}$ specifies the minimum collector–emitter voltage required to drive the transistor in the active region. The area enclosed by dotted lines represents the safe operating area of the transistor.

$P_{D(max)}$ is usually specified at a given ambient temperature and it should be derated at higher temperatures as per the derating curve supplied by the manufacturers. The use of heat sink results in increased power dissipation capability of the transistor. The actual dissipation capability can be determined from known values of maximum operating junction temperature, ambient temperature and the thermal resistance involved. There are two types of thermal resistances associated with a transistor: the junction-to-case thermal resistance and the case-to-ambient thermal resistance. The former tells about how effectively heat is conducted away from the junction to the case, and the latter tells about how effectively the heat is conducted away from the case to ambient.

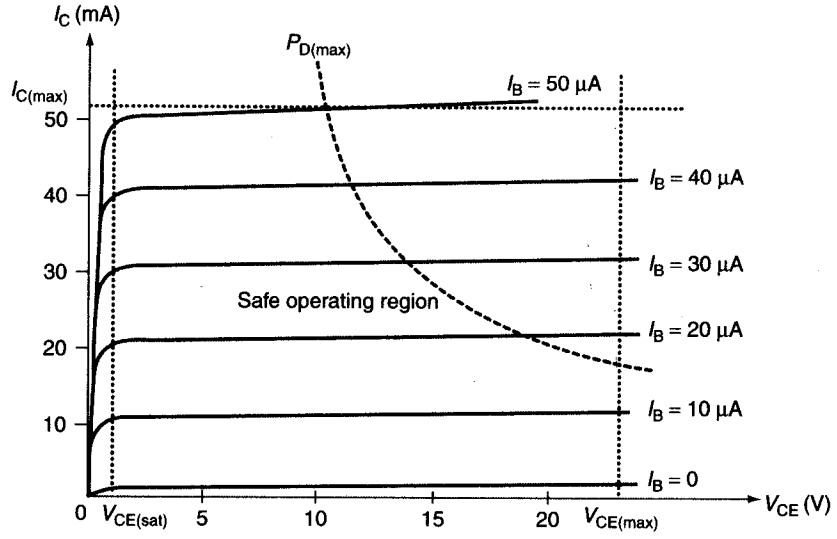


Figure 3.20 | Maximum ratings of a transistor.

Table 3.2 | Typical transistor applications and important specifications

S. No.	Application requirements	Important specifications
1.	General purpose, low-level amplifier and switching transistors	h_{FE}, $I_{C(max)}$, f_T, V_{CEO}
2.	Power-switching applications	V_{CEO}, V_{CBO}, h_{FE}, $I_{C(max)}$, f_T, $P_{D(max)}$
3.	Low-level IF/RF amplification	$I_{C(max)}$, f_T, V_{CEO}
4.	Audio amplification	h_{FE}, $I_{C(max)}$, $P_{D(max)}$, V_{CEO}
5.	High-voltage transistors	V_{CEO}, V_{CBO}, h_{FE}, $I_{C(max)}$, f_T

The case-to-ambient thermal resistance depends upon the transistor's package size. It is, for instance 300°C/W for TO-18 package, 150°C/W for TO-5 and TO-39 packages, 60°C/W for TO-66 package and only 30°C/W for TO-3 package. The effective case-to-ambient thermal resistance can be reduced by using an appropriate heat sink that basically increases the effective radiating area.

All specifications are not equally important for all application requirements. Table 3.2 lists some typical applications and the corresponding transistor parameters that would significantly affect the choice criteria.

3.9 Lead Identification

Bipolar junction transistors are made in a large variety of package styles. Some of the more popular package styles include the TO-5, TO-18, TO-39, TO-72, TO-237, TO-92, TO-3, TO-66 and TO-220 packages. Transistors in TO-3 and TO-66 packages are high-power devices, while those with small metal can or plastic body (TO-5, TO-18, TO-39, TO-72, TO-237, TO-92, TO-220) are low- to medium-power devices. Transistor leads are made of gold, aluminum or nickel and then encapsulated in a container. The lead arrangement for different transistor package styles is shown in Figure 3.21.

It is interesting to note that the lead arrangement of different types of transistors with varying current and voltage specifications, manufactured by different companies is identical only if these devices happen to have the same package style, except some packages such as TO-92 and TO-106 where different lead arrangements are possible for different type numbers having the same package style. For instance, transistors 2N3055 and BU205 have the same lead arrangements as both these transistors are made in TO-3 package though they have widely different electrical specifications and application areas, with the former being a low-voltage power-switching transistor and the latter being a high-voltage transistor. Similarly, transistor type numbers SL/CL100 and 2N2218 made in TO-39 package too have identical terminal arrangements though the former is an audio transistor and the latter is a low-power switching transistor.

On the other hand, transistors 2N370H and 2N5401 are both made in TO-92 package but have different lead arrangements. Another interesting point to note here is that the terminal identification does not change with the change in polarity of the transistor (i.e., whether it is a PNP or an NPN transistor), as long

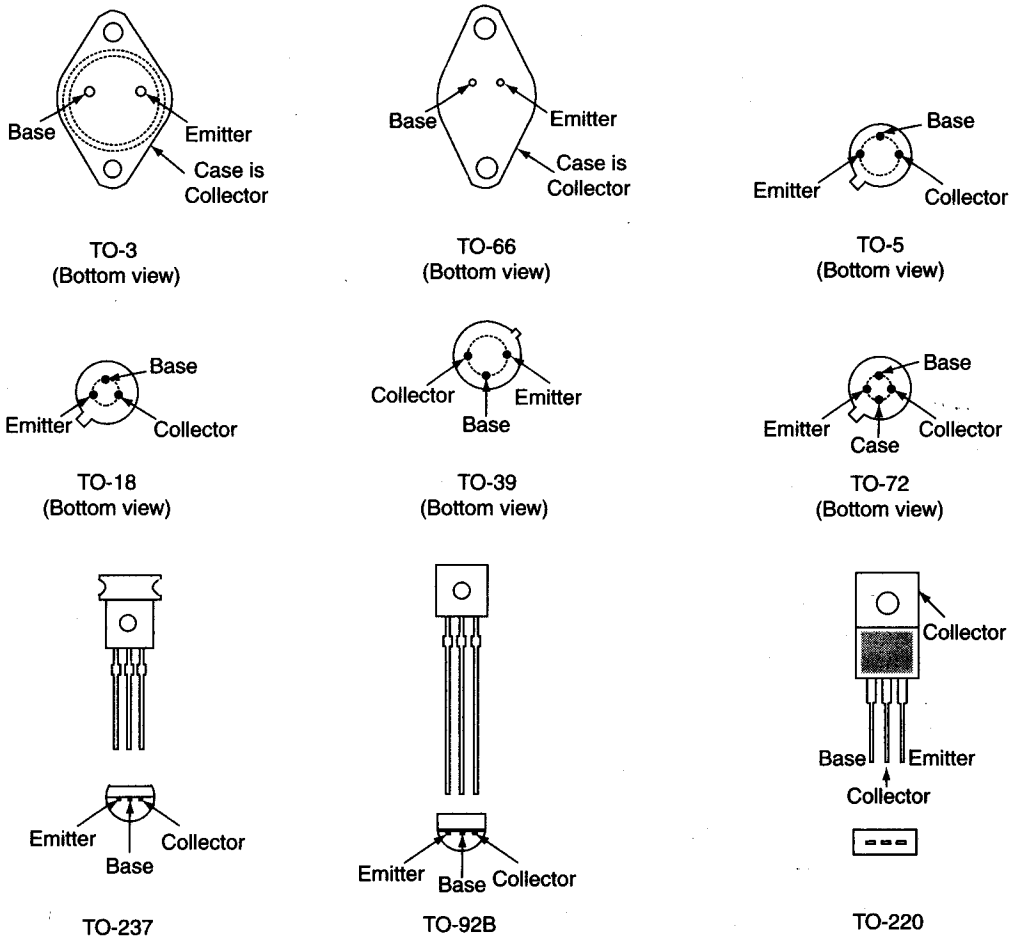


Figure 3.21 | Transistor package styles and lead identification.

as the package is the same. For instance, transistor type numbers 2N2222 and 2N2907 have the same lead arrangements though the former is an NPN transistor and the latter is a PNP transistor.

Remembering the lead arrangement of different transistor package styles becomes simple if we take into account of the following points

1. Metal can transistor packages (TO-5, TO-18, TO-39) invariably have a notch and the lead adjacent to the notch is the emitter. The leads are identified as emitter–base–collector starting from the emitter and moving clockwise.
2. The collector is usually connected internally to the metal can in such packages. One can easily identify the lead that is common to the metal body by careful observation and even a continuity check with the multimeter is not needed.
3. In some of the plastic packages like TO-106 for instance, there is a dot near the emitter lead.
4. The lead arrangements of TO-66 and TO-3 package styles are identical when both types are viewed in the same way. The metal body in both these types is the collector and there is no separate lead for the collector.
5. Transistors with TO-72 package have four leads with the fourth lead connected to the case internally. The package has a notch near the emitter lead and the leads are identified as emitter–base–collector starting from the emitter and moving clockwise just like other similar packages with a notch but having three leads.
6. Another widely used package designation for the transistors is the "SOT" designation, which has much larger number of package styles than the popular "TO" designation. But for most of the popular transistor numbers there is a corresponding "TO" designation for a given "SOT" designation and vice versa. For example, SOT-18 is nothing but TO-72 and SOT-54 is the same as TO-92 package. Also, there are some popular SOT packages that are only a slight variation of the popular TO packages, for example SOT-93 is similar to TO-220 but with a slightly larger width. As far as lead identification is concerned, for a given SOT package, it is the same as that for the corresponding TO package.
7. RF power transistors are packaged in different styles when compared with conventional power transistors. The popular package styles in this category are SOT-119, SOT-120, SOT-121, SOT-122 and SOT-123 (Figure 3.22). Identifying the leads of these transistors is quite straight forward. Packages SOT-120 to SOT-123 are more or less identical except for a slight variation in dimensions. Each one of them has four strips (leads in RF power transistors are in the form of strips) placed 90° with respect to each other over a 360° circle. The strip with a slight angular cut is always the collector and the strip opposite to the collector is always the base. The other two strips are both emitters. In SOT-119, there are six strips out of which the four outer ones are all emitters, the smaller of the two middle ones is always the collector and the remaining one is the base.

Transistor leads can also be identified using a multimeter. The procedure for identifying the leads is the same as that for PN junction diodes. The collector–base and emitter–base junctions can be checked with the multimeter to identify the leads. But such a test gives the correct result only if the device under test is healthy.

In the multimeter identification of transistor leads, if either the collector or the emitter lead is known, the other two leads can be identified without any problem from a single junction test. If the emitter terminal is known (emitter is the terminal adjacent to the notch in TO-5, TO-18, TO-39, TO-72 package styles) then the base and the collector terminals are identified by performing the collector–base diode junction test. If the collector terminal is known (it is usually connected to the body in the case of TO-5, TO-18, TO-39, TO-72 package styles and is in fact the body in case of TO-66 and TO-3 packages) then the base and the emitter terminals can be identified by taking the emitter–base junction diode test. Also, whether the transistor is an NPN or a PNP transistor, the meter shows an open circuit between the collector and the emitter terminals in both the directions.

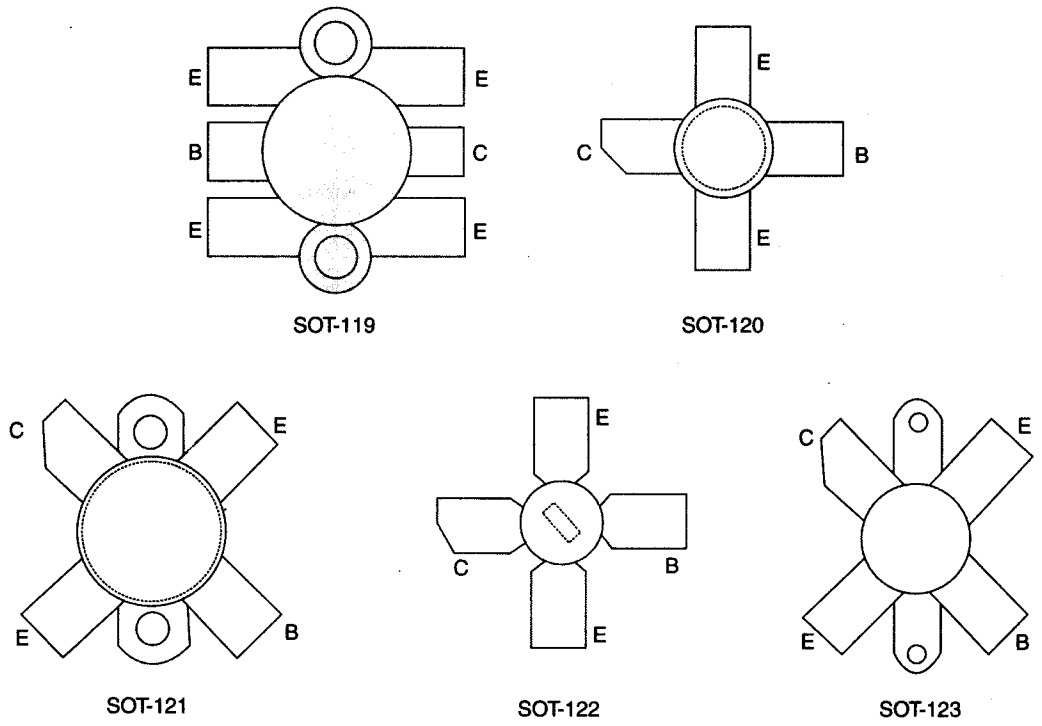


Figure 3.22 | Package styles and lead identification of RF transistors.

The multimeter tests for identifying the leads of a bipolar junction transistor are illustrated in Figures 3.23(a)–(f) for an NPN transistor and in Figures 3.24(a)–(f) for a PNP transistor. The test arrangements depicted in these figures are self-explanatory.

3.10 Transistor Testing

As in case of diodes, transistors also can be checked using a multimeter, an ohmmeter and a curve tracer. Using a multimeter, transistors are tested by checking the emitter–base and collector–base junctions in the same fashion as explained in the case of the PN junction diode. The junction must be tested both in the forward-biased and reverse-biased modes. As an example, in case of an NPN transistor the emitter–base junction is forward-biased by connecting the red lead of the multimeter to the base and the black lead to the emitter. In the case of a healthy transistor, the multimeter will show the voltage corresponding to the forward voltage drop of the emitter–base junction when set to the diode test position. An OPEN reading in this condition indicates a faulty transistor. The emitter–base junction is reverse-biased by interchanging the connections and now the meter should show an OL (open) reading. A short circuit or a low resistance in this case indicates a faulty transistor. Similarly, the collector–base junction can also be checked. In addition, collector–emitter terminals should show an open condition in both the directions.

Advanced digital meters provide the value of h_{fe} by placing the transistor in the socket provided for the purpose. The diode-testing mode provided in these meters can be used to check whether the transistor is working properly or not.

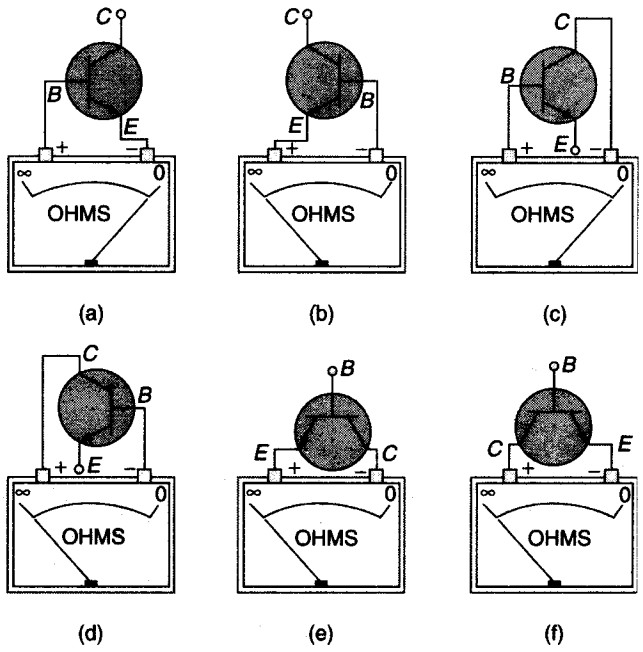


Figure 3.23 | Lead identification of NPN transistors using a multimeter.

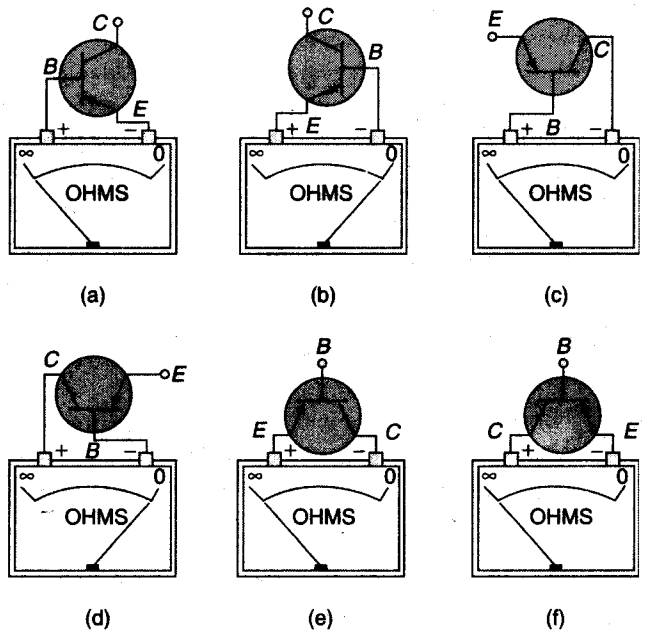


Figure 3.24 | Lead identification of PNP transistors using a multimeter.

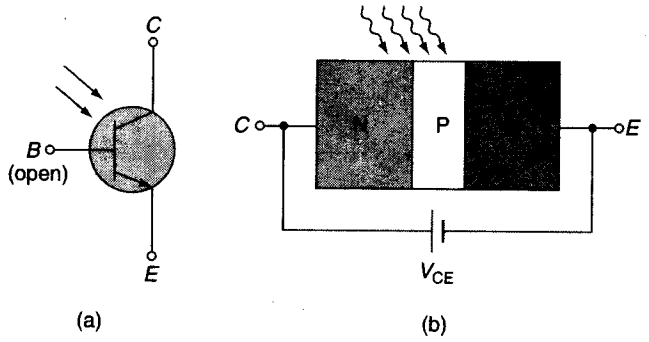


Figure 3.25 | (a) Circuit symbol for phototransistors; (b) phototransistor connection.

Transistors can be checked using an ohmmeter or the resistance scale of digital multimeters. With the collector open, forward biasing the emitter–base junction should show a low resistance and reverse biasing the emitter–base junction should show an OL (open) condition. Similarly, with emitter open, the collector–base junction can be checked.

Curve tracer can be used for comprehensive testing of transistors as it can be used to display the input and output characteristics of a transistor. The value of transistor β or h_{fe} can be calculated from these curves.

3.11 Phototransistors

Phototransistors are solid-state light sensors that possess internal gain. Phototransistors can be viewed as photodiodes whose output current is fed to the base of a conventional small signal transistor. Figure 3.25(a) shows the circuit symbol of a phototransistor and Figure 3.25(b) shows its connection diagram. Phototransistor gain is of the order of 100–1500 as compared to unity gain of photodiodes. Although the output of photodiodes can be amplified through the use of an external operational amplifier, phototransistors offer a cost-effective option. However, the response time of phototransistors is of the order of few to hundreds of microseconds, which is much larger than that of photodiodes.

Phototransistors are discussed in detail in the chapter on optoelectronic devices (Chapter 7).

3.12 Power Transistors

Power transistors, as the name suggests, are transistors intended for high-power applications. Improvements in production techniques have resulted in higher transistor power ratings in smaller packages with increased breakdown voltages and faster switching times.

The power handling capability of the transistor and the collector junction temperature are related to each other as the power dissipated by the device causes an increase in the junction temperature of the transistor. The average power dissipated in a transistor is given by the expression

$$P_D = V_{CE} \times I_C \tag{3.26}$$

The maximum power rating ($P_{D(max)}$) is defined as the maximum power that can be safely dissipated in a transistor. The transistor can dissipate this power up to a certain case temperature. Above this temperature the power handling capability of the transistor decreases with increase in the case temperature and becomes zero at the maximum operating temperature (Figure 3.26). Silicon transistors have higher operating temperatures as compared to germanium transistors with typical maximum values for the junction temperatures being 150–200°C for silicon transistors and 100–110°C for germanium transistors.

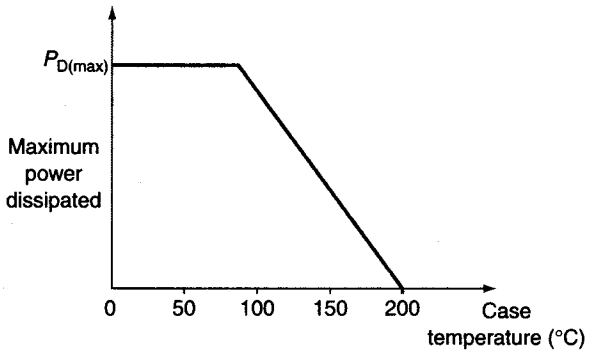


Figure 3.26 | Power derating curve of a transistor.

Power transistors are mounted on large metal cases called heat sinks to provide a large area for better radiation of heat. With the heat sink, the transistor has a larger area from which to radiate the heat into the air, thereby holding the case temperature to a much lower value than would be possible without the heat sink.

Let us now consider how the transistor junction temperature (T_J), the case temperature (T_C) and the ambient temperature (T_A) are related to the power handling capability of the power transistor. One of the most important parameters that defines the power handling capability of any device is its thermal resistance. It provides information about how much temperature change occurs for a given amount of power dissipation. Thermal resistance is measured in °C/W. Lower the value of the thermal resistance of the device more is its power handling capability. The temperature of the transistor junction is given by the formula

$$T_J = P_D\theta_{JA} + T_A \tag{3.27}$$

where T_J is the transistor junction temperature, P_D the power dissipated in the transistor, θ_{JA} the junction-ambient thermal resistance and T_A the ambient temperature.
Also

$$T_J = P_D\theta_{JC} + T_C \tag{3.28}$$

where θ_{JC} is the junction-case thermal resistance and T_C the case temperature.

Without the heat sink the typical value of θ_{JA} ($\theta_{JC} + \theta_{CA}$) is in the range of 40–50°C/W (θ_{CA} is the case–ambient thermal resistance), and with the heat sink the value of θ_{JA} ($\theta_{JC} + \theta_{CS} + \theta_{SA}$) is reduced to around 2–5°C/W (θ_{CS} is the case-heatsink thermal resistance; θ_{SA} is the heatsink-ambient thermal resistance). Thus, the use of heat sink results in reduced value of transistor junction to ambient thermal resistance and increase in power dissipation capability of the transistor.

EXAMPLE 3.5

What should be the maximum value of junction-to-case thermal resistance of a certain silicon transistor that has a maximum junction operating temperature of 200°C and that can safely dissipate a power of 300 W at a case temperature of 25°C.

Solution

1. The said transistor can safely dissipate a power of 300 W at a case temperature of 25°C. Therefore, maximum allowable junction-case temperature differential is (200–25) = 175°C.
2. Therefore, the maximum value of junction-to-case thermal resistance = 175/300 = 0.583°C/W.

Answer: Maximum value of junction-to-case thermal resistance is 0.583°C/W.

EXAMPLE 3.6

A silicon transistor has junction-to-case and junction-to-ambient thermal resistances of 10°C/W and 100°C/W, respectively. The maximum junction temperature is 200°C. Determine the power dissipation capability of a transistor:

1. *When operating at a case temperature of 50°C.*
2. *When the ambient temperature is 25°C.*

Solution

1. When the case temperature is 50°C, the maximum allowable junction-case temperature difference is 150°C. This gives power dissipation capability as 150/10 = 15 W.
2. Maximum allowable temperature difference between ambient and junction = 175°C.

   Ambient-junction thermal resistance = 100°C/W

   This gives power dissipation capability as 175/100 = 1.75 W

Answer: The power dissipation capability of transistor is (1) 15 W and (2) 1.75 W.

3.13 Transistor Construction Techniques

Transistors can be constructed using various techniques, the important ones being point contact, grown-junction, alloy-junction, diffusion, epitaxial and annular techniques.

Point-Contact Transistors

The earliest transistors fabricated were point-contact transistors. Point-contact transistors are constructed by placing two wires into the semiconductor wafer. The wires are N-type and the wafer is P-type for an NPN transistor (Figure 3.27) and vice versa for a PNP transistor. PN junction is formed between the wire and the wafer by applying electrical pulses to each of the wire. These transistors suffer from poor reliability and are no longer used.

Grown-Junction Type Transistors

Grown-junction type transistors are fabricated from a single crystal. The crystal is drawn from a melt of silicon or germanium whose impurity concentration is changed by adding the N-type and the P-type dopants during the crystal drawing operation. The crystal is then sliced into a large number of devices and the contacts are then made (Figure 3.28).

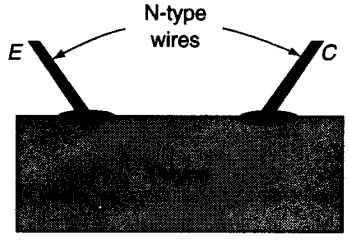


Figure 3.27 | Point-contact transistors.

Figure 3.28 | Grown-junction type transistors.

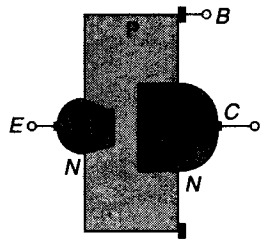


Figure 3.29 | Alloy-junction transistors.

Alloy-Junction Transistors

In the case of alloy-junction transistors, the base is a thin wafer. Two dots of impurity elements are placed on opposite sides of this wafer. In the case of an NPN transistor the wafer is a P-type material and the dots are of N-type material (Figure 3.29), whereas in the case of PNP transistors the wafer is an N-type material and the dots are of P-type material. The whole structure is raised for a short time to a temperature high enough to melt the impurity into the base material. As is clear from Figure 3.29, the collector region is made larger than the emitter region. This is done so that the collector region collects maximum number of majority carriers from the emitter region and prevents them from diffusing into the base region.

Diffusion Transistors

The most frequently used technique for transistor fabrication is the diffusion technique. In this technique the semiconductor wafer is subjected to gaseous diffusions of both N-type and P-type impurities to form the emitter–base and the collector–base junctions. Two types of transistors are fabricated using the diffusion technique, namely, the planar transistors and the mesa transistors. The planar NPN silicon transistor of the diffusion type is shown in Figure 3.30(a). The collector–base region is photo-etched on the block of N-type silicon and a P-type base region is formed by a gaseous diffusion-masking process. The emitter is then diffused onto the base and the whole structure is covered by a layer of silicon oxide.

Mesa transistor is essentially a planar transistor that has been etched at the collector–base junction leaving a mesa or a flat-topped peak [Figure 3.30(b)]. Mesa transistors are rugged devices with high power-dissipation capability and can operate at higher frequencies. However, they have higher value of saturation voltage because of highly resistive collector region. Hence, they are unsuitable for switching applications.

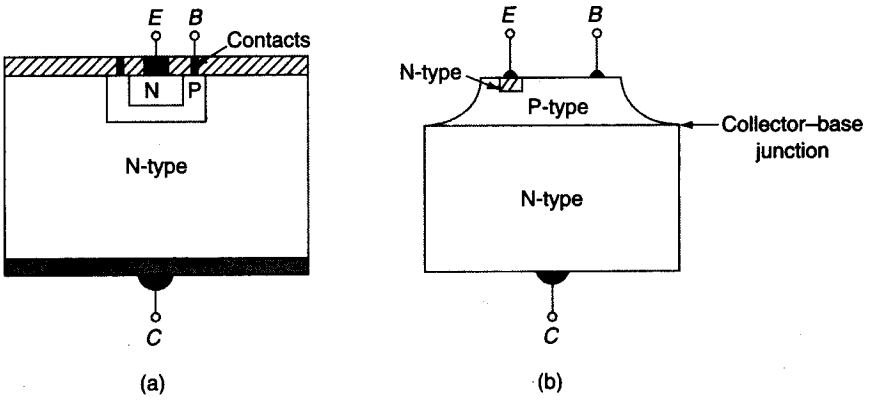


Figure 3.30 | (a) Planar diffusion transistors; (b) mesa diffusion transistors.

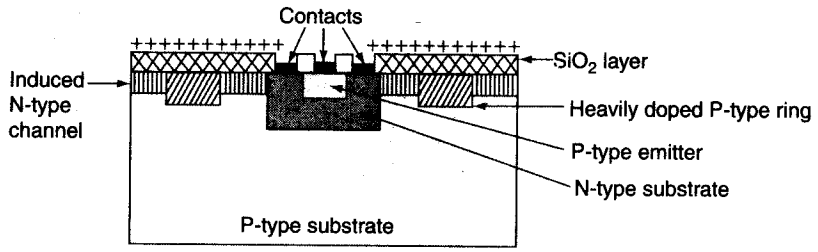


Figure 3.31 | Annular transistors.

Epitaxial Transistors

The epitaxial technique consists of growing a very thin, high purity, single-crystal layer of silicon or germanium on a heavily doped substrate of the same material. This augmented crystal forms the collector on which the base and the emitter regions are diffused. Both planar and mesa transistors can be constructed using this technique.

Annular Transistors

In annular transistors, a heavily doped ring is introduced around the base region. The ring is of the P-type material for PNP transistors (Figure 3.31) and of the N-type for NPN transistors. It interrupts the induced channel and isolates the collector–base junction from the surface of the device. It is therefore a high-voltage device with low collector–base leakage.

KEY TERMS

AC current gain (h_{fe})
Active region
Alloy-junction transistors
Alpha (α)
Annular transistors
Base-spreading resistance ($r_{bb'}$)
Beta (β)
Common-collector configuration
Common-emitter configuration
Common-base configuration
Diffusion technique
Early effect
Ebers–Moll transistor model
Epitaxial technique
Gain-bandwidth product (f_T)
Grown-junction transistor
$I_{C(max)}$
Mesa transistor
NPN transistor
PNP transistor
Point-contact transistors
Reach-through or the punch-through effect
Reverse-active region
Saturation region
Transistor

OBJECTIVE-TYPE EXERCISES

Multiple-Choice Questions

1. A semiconductor transistor operates in the active region only when
   a. the emitter–base junction is forward-biased and the collector–base junction is reverse-biased.
   b. both emitter–base and collector–base junctions are forward-biased.
   c. both emitter–base and collector–base junctions are reverse-biased.

d. the collector-base junction is forward-biased and emitter-base junction is reverse-biased.

2. Which of the following is/are metal can package/s:
   a. TO-5
   b. TO-18
   c. TO-92
   d. Both (a) and (b)

3. When a healthy NPN transistor is connected to an ohmmeter such that the base terminal is connected to the red lead of the meter and the emitter terminal to the black lead then the meter shows
   a. an open circuit.
   b. some medium resistance.
   c. a very small resistance.
   d. none of the above.

4. A conducting bipolar transistor dissipates least power when operating in the
   a. saturation region.
   b. cut-off region.
   c. active region.
   d. reverse-active region.

5. A bipolar transistor in sinusoidal oscillator configuration is operating in the
   a. active region.
   b. saturation region.
   c. cut-off region.
   d. reverse-active region.

6. The maximum reverse collector to emitter breakdown voltage with base open is referred to as
   a. V_{CEO}
   b. V_C
   c. V_{CBO}
   d. V_{EBO}

7. When a transistor is used as a switch, the base current required to switch on the transistor for a given collector current is calculated from
   a. h_{fe}
   b. α
   c. γ
   d. σ

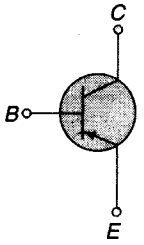
8. For $\alpha = 0.9$ the value of β is
   a. 1
   b. 0.9
   c. 9
   d. 10

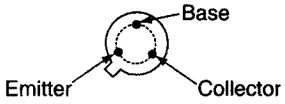
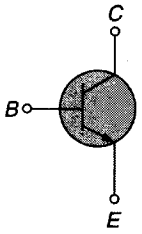
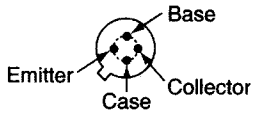
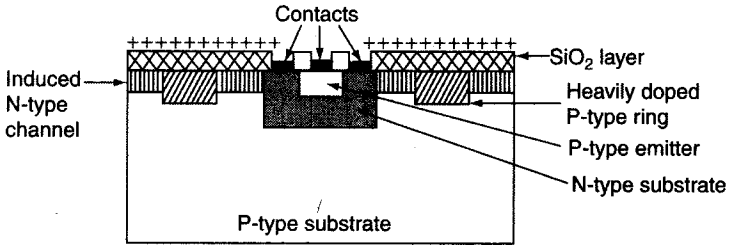
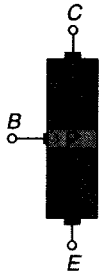
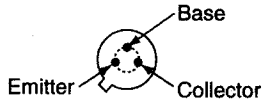
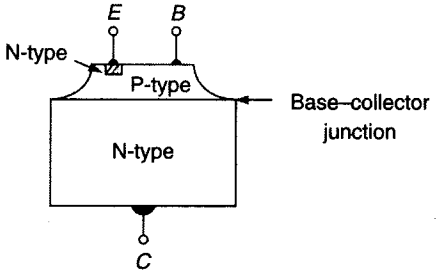
9. With increase in the collector-base reverse voltage
   a. the base width increases.
   b. the base width decreases.
   c. the base width is not affected.
   d. the base width can increase or decrease.

10. Which of the transistor configurations is capable of providing both voltage and current gains?
    a. Common base
    b. Common collector
    c. Common emitter
    d. Both common emitter and common base

Match the Following

Match the terms in Column (a) with the figures in Column (b).

S. No.	Column (a)	S. No.	Column (b)
1.	NPN transistor	A.	

2.	TO-5 package	B.	
3.	TO-18 package	C.	
4.	Annular transistor	D.	
5.	Diffused Mesa transistor	E.	
		F.	
		G.	
		H.	

REVIEW QUESTIONS

1. "*Transistors are current-controlled devices, whereas vacuum triodes are voltage-controlled devices.*" Comment.
2. Draw the structure of NPN and PNP transistors showing the direction of flow of currents through the transistor.
3. Explain the principle of operation of a PNP transistor in the active region?
4. Sketch the typical input and output characteristics of a bipolar transistor when connected in
   a. Common-emitter configuration.
   b. Common-base configuration.

   Also derive the relationship between α and β.
5. Define and interpret the following transistor ratings and specifications:
   a. V_{CBO}
   b. V_{CEO}
   c. $P_{D(max)}$
   d. α
6. Explain in detail the early effect phenomenon. How does it affect the transistor characteristics?
7. Explain the operation of a transistor using the Ebers–Moll model?
8. Compare the common-base, common-emitter and common-collector configurations of a transistor?
9. Explain the manufacturing process for diffused mesa and annular transistors. Give one merit and one demerit for each configuration.
10. How will you identify the terminals of a transistor using
    a. an ohmmeter?
    b. a multimeter?
11. List any four differences in the characteristic curves of silicon and germanium transistors.
12. Give reasons for the following:
    a. Why is the collector current slightly less than the emitter current?
    b. Why is a transistor referred to as a bipolar junction device?
    c. The power rating of a transistor decreases with increase in the ambient temperature.
    d. The concentration of minority carriers in the base region increases with increase in the reverse-bias voltage of the collector–base junction.

PROBLEMS

1. A transistor with $\alpha = 0.97$ has a reverse saturation current of 1 μA in the common-base configuration. Calculate the value of leakage current in the common-emitter configuration. Also find the collector current and the emitter current if the value of base current is 20 μA.
2. Figure 3.32 shows the input characteristics of a common-emitter transistor. Find the input resistance for the linear portion of the curves for collector–emitter voltages of 1 and 20 V.
3. For the circuit in Figure 3.33, determine the value of R_1, given that $V_{BE} = 0.7$ V, $I_{CO} = 0$.
4. For the circuit in Figure 3.34, find the voltage across the load resistance R_L, given that $V_{BE} = 0.7$ V, $\alpha = 0.98$, $I_{CO} = 0$.

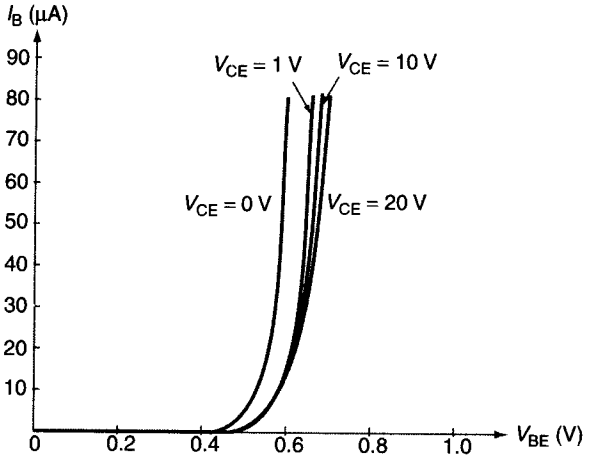


Figure 3.32 | Problem 2.

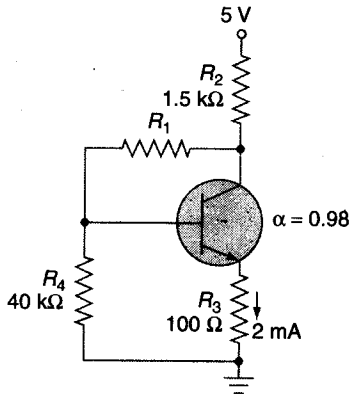


Figure 3.33 | Problem 3.

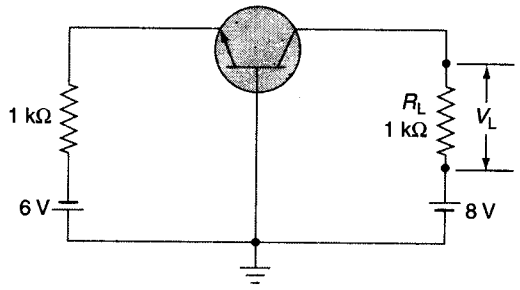


Figure 3.34 | Problem 4.

ANSWERS

Multiple-Choice Questions

1. (a)
2. (d)
3. (c)
4. (a)
5. (a)
6. (a)
7. (a)
8. (c)
9. (b)
10. (c)

Match the Following

1. C
2. B
3. G
4. E
5. H

Problems

1. 33.33 μA; 0.68 mA; 0.7 mA
2. 666.67 Ω; 1500 Ω
3. 17.12 kΩ
4. 5.2 V

CHAPTER 4

Transistor Biasing and Thermal Stabilization

Learning Objectives

After completing this chapter, you will learn the following:

- Importance of transistor biasing.
- Designing a transistor-biasing circuit.
- Detailed analysis of fixed-bias, emitter-bias, collector-to-base-bias and voltage-divider-bias with emitter-bias configurations.
- Design of common-base and common-collector configurations.
- Understanding the importance of stability factors $S_{I_{CO}}$, S_{β} and $S_{V_{BE}}$.
- Derivation of expressions for stability factors for different biasing configurations.
- Phenomenon of thermal runaway.
- Bias compensation techniques.
- Operation of transistor as a switch.

In the last chapter the fundamentals of transistor construction and operation were discussed. After understanding the fundamentals of transistor operation, we are in a position to design a transistor-based amplifier circuit. The design of any electronic amplifier involves two important aspects, namely, the DC response and the AC response. The choice of parameters to establish the desired DC levels affect the AC response and vice versa. The DC analysis and the AC analysis are done separately and then superposition theorem is applied for the complete analysis.

To design a transistor-based amplifier circuit it is necessary to operate the transistor in the active region. This is done using a transistor-biasing circuit. This chapter focuses on the importance of transistor biasing and the various transistor-biasing configurations including fixed-bias, emitter-bias, collector-to-base-bias and voltage-divider-bias with emitter-bias configuration. The stability offered by each of the configurations against variations in temperature and other parameters is another topic covered in the chapter. Towards the end of the chapter, the phenomenon of thermal runaway and design of transistor switch is covered.

4.1 Operating Point

We have studied in Chapter 3 that a transistor acts as an amplifier when it is operated in the active region of its output characteristics. Therefore, the first step in designing a transistor amplifier is to design a circuit so as to enable the transistor to operate in its linear active region. This is done by using external components

such as resistors and capacitors and applying DC voltages to the transistor so as to establish proper collector current (I_C) and collector–emitter voltage (V_{CE}) across the transistor. This process is referred to as *transistor biasing* and the circuit used for transistor biasing is called a *biasing circuit.* Transistor biasing is done so that the transistor amplifies the input signal linearly and without distortion.

There are four conditions that should be met for a transistor to act as a faithful amplifier. First, the emitter–base junction should be forward-biased and the collector–base junction should be reverse-biased for all levels of input signal. For the emitter–base junction to be forward-biased, the base–emitter voltage (V_{BE}) should not fall below 0.3 V for germanium transistors and below 0.7 V for silicon transistors for all values of input signal. Second, the collector–emitter voltage (V_{CE}) should not fall below the knee voltage ($V_{CE(sat)}$) for any part of the input signal. For V_{CE} less than the $V_{CE(sat)}$ (0.5 V for germanium transistor and 1.0 V for silicon transistor), the collector–base junction is not properly reverse-biased. Third, the value of collector current (I_C) when no signal is applied should be at least equal to the maximum collector current due to signal alone. Finally, the maximum ratings of the transistor ($I_{C(max)}$, $V_{CE(max)}$ and $P_{D(max)}$) should not be exceeded at any value of the input signal.

The DC collector current (I_C) and the collector–emitter voltage (V_{CE}) when no input signal is applied are collectively referred to as the *operating point.* Since the operating point is a fixed point on the output characteristics of the transistor, it is also referred to as the *quiescent point* (Q-point). Judicious selection of the operating point is important for faithful amplification of the input signal. Figure 4.1 shows the output characteristics of a common-emitter amplifier with four different operating points. The functioning of the transistor amplifier for each of these operating points is discussed in the following paragraphs. This will help in understanding the importance of selecting the correct operating point.

Operating point A represents a condition when no bias is applied to the transistor. The transistor is in the cut-off region and there is no collector current through the transistor. Also, the base–emitter voltage is zero. It does not satisfy any of the conditions necessary for faithful amplification and hence A is not a suitable operating point.

Point B would allow some positive and negative variations of the output signal but the peak-to-peak output voltage is limited due to the proximity of the operating point to the knee point ($V_{CE(sat)}$). Also, non-linearities will be introduced in the amplification as the spacing between the I_C curves is not linear near the knee region.

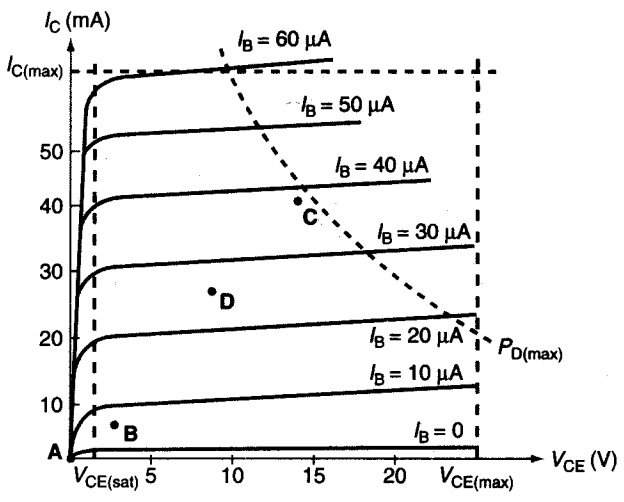


Figure 4.1 | Selecting a suitable operating point.

Point C is too close to the $P_{D(max)}$ curve of the transistor. Therefore, the output voltage swing in the positive direction is limited.

Point D is located in the middle of the active region of the transistor characteristics. It will allow both the positive and the negative excursions in the output signal. It also provides linear gain and largest possible output voltage and current swing. Therefore, the operating point for a transistor amplifier is selected to be in the middle of the active region.

It may be mentioned here that after having selected the operating point, the effect of temperature should also be taken into account. A rise in the temperature results in increase in the value of transistor gain (β) and the leakage current (I_{CO}). This results in a shift in the operating point. The biasing network should also provide temperature stability so that there is minimum variation in the operating point with change in temperature. The concept of bias stabilization is discussed in detail in Section 4.5.

4.2 Common-Emitter Configuration

Common-emitter configuration is the most popular of the three transistor amplifier configurations because it offers considerable current gain as well as voltage gain. There are several common-emitter biasing circuits, namely the fixed-bias, emitter-bias, voltage-divider-bias with emitter-bias and collector-to-base-bias circuits. The various biasing circuits are discussed in detail in this section. Also DC analysis, load-line analysis and merits and demerits of each of the configurations are covered.

Fixed-Bias Circuit

Consider the circuit shown in Figure 4.2. It is referred to as the fixed-bias circuit and is one of the simplest possible transistor-biasing circuits. The biasing components include two resistors, base resistor (R_B) and collector resistor (R_C), and a supply voltage (V_{CC}). The base–emitter junction gets forward-biased through V_{CC} and R_B. The supply voltage also reverse biases the collector–base junction through resistor R_C. Resistor R_B is of the order of few hundreds of kilo-ohms whereas typical value of R_C is of few kilo-ohms. Capacitors C_i and C_o are referred to as the input and the output coupling capacitors, respectively.

DC Analysis

DC analysis of a circuit refers to analyzing a circuit so as to establish the operating point in the absence of any input AC signal. For the purpose of DC analysis, the input and output capacitors are considered as open and it is assumed that all AC sources are zero (Figure 4.3).

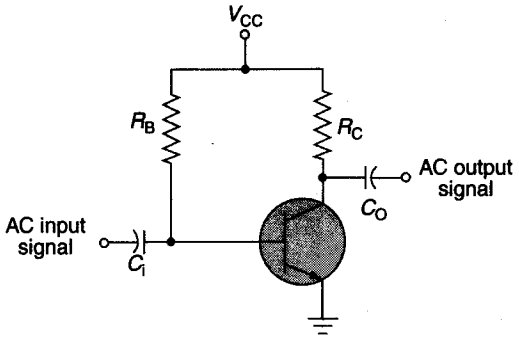


Figure 4.2 | Fixed-bias circuit.

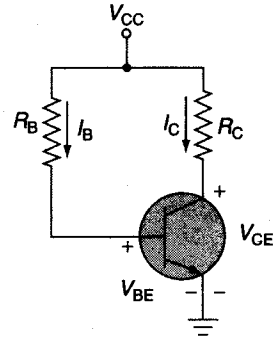


Figure 4.3 | DC equivalent of fixed-bias circuit.

Before going into detailed analysis of the circuit, let us discuss the notations used in the chapter. Base–emitter voltage is the voltage at the base terminal with respect to the emitter terminal or the base–emitter differential voltage. It is denoted by V_{BE} and is given by

$$V_{BE} = V_B - V_E \tag{4.1}$$

where V_B is the base voltage wrt ground; V_E the emitter voltage w.r.t. ground.

Collector–emitter voltage is the voltage at the collector terminal w.r.t. the emitter terminal or the collector–emitter differential voltage. It is denoted by V_{CE} and is given by

$$V_{CE} = V_C - V_E \tag{4.2}$$

where V_C is the collector voltage wrt ground; V_E the emitter voltage w.r.t. ground.

The base–emitter section of the fixed-bias circuit comprises the supply voltage (V_{CC}), the base resistor (R_B) and the transistor base–emitter junction. Base current (I_B) can be determined by applying Kirchhoff's voltage law to the base–emitter section:

$$V_{CC} - I_B R_B - V_{BE} = 0 \tag{4.3}$$

Rearranging the terms in Eq. (4.3) we get the value of base current (I_B) as

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{4.4}$$

From Eq. (4.4) it is clear that the base current (I_B) is given by ratio of the voltage drop across the base resistor (R_B) to the value of R_B. The value of base–emitter voltage (V_{BE}) is small as compared to the supply voltage (V_{CC}) and hence can be neglected without causing much error. Therefore, Eq. (4.4) can be approximated as

$$I_B \cong \frac{V_{CC}}{R_B} \tag{4.5}$$

The collector current (I_C) of the transistor is directly related to the base current (I_B) and is expressed as

$$I_C = \beta I_B$$

that is

$$I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right) \cong \frac{\beta V_{CC}}{R_B} \tag{4.6}$$

where β is the transistor current gain.

We can infer from Eq. (4.6) that the collector current (I_C) is dependent on the supply voltage (V_{CC}) and the base resistor (R_B) and is independent of the value of collector resistor (R_C). Any change in the value of R_C will not have any effect on the base current or the collector current as long as the transistor is operating in the active region. However, the transistor collector–emitter voltage (V_{CE}) depends on the value of R_C.

The collector–emitter section comprises the supply voltage (V_{CC}), collector resistor (R_C) and the transistor collector–emitter junction. Applying Kirchhoff's voltage law to the collector–emitter section we get

$$V_{CC} - I_C R_C - V_{CE} = 0 \tag{4.7}$$

Rearranging the terms we get

$$V_{CE} = V_{CC} - I_C R_C \tag{4.8}$$

Thus, the collector–emitter voltage (V_{CE}) is equal to the difference between the supply voltage (V_{CC}) and the voltage across the collector resistor (R_C).

The values of collector current (I_C) and collector–emitter voltage (V_{CE}) given in Eqs. (4.6) and (4.8) represent the operating point or the quiescent point and are denoted as I_{CQ} and V_{CEQ}, respectively. The quiescent point for a fixed-bias circuit is given by

$$I_{CQ} = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right), \quad V_{CEQ} = V_{CC} - I_{CQ}R_C \tag{4.9}$$

Load-Line Analysis

The expression given in Eq. (4.8) relates to two variables, namely, the collector current (I_C) and the collector–emitter voltage (V_{CE}). The transistor output characteristics curve also relates these two variables. If we superimpose the straight line defined by Eq. (4.8) on the transistor output characteristics, we can determine the operating point of the circuit and also how the operating point changes with change in the value of circuit parameters. This is referred to as load-line analysis (Figure 4.4).

To draw the load line, substitute $I_C = 0$ in Eq. (4.8). We get

$$V_{CE} = V_{CC}\big|_{I_C = 0}$$

This point appears on the horizontal axis (0, V_{CC}) of the output characteristics. I_C can be evaluated by substituting $V_{CE} = 0$ in Eq. (4.8) as

$$I_C = \frac{V_{CC}}{R_C}\bigg|_{V_{CE} = 0}$$

This point appears on the vertical axis (V_{CC}/R_C, 0) of the output characteristics.

The load line is obtained by joining these two points as shown in Figure 4.4. The operating point is established on the load line by determining the level of base current (I_B) using Eq. (4.4) or Eq. (4.5). The point of intersection of the load line with the curve corresponding to the calculated value of I_B gives the operating point as shown in the figure. The operating point shifts with the change in the value of circuit parameters.

The operating point moves up the load line if the value of I_B increases and moves down the load line when the value of I_B decreases (Figure 4.5). The value of I_B can be changed by changing the value of resistor

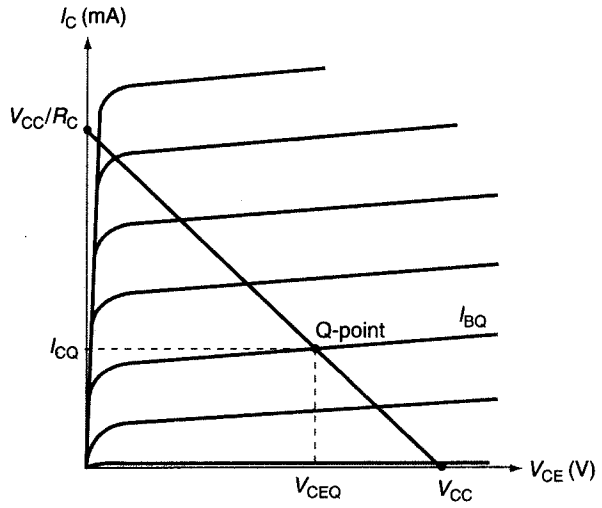


Figure 4.4 | Load-line analysis of the fixed-bias circuit.

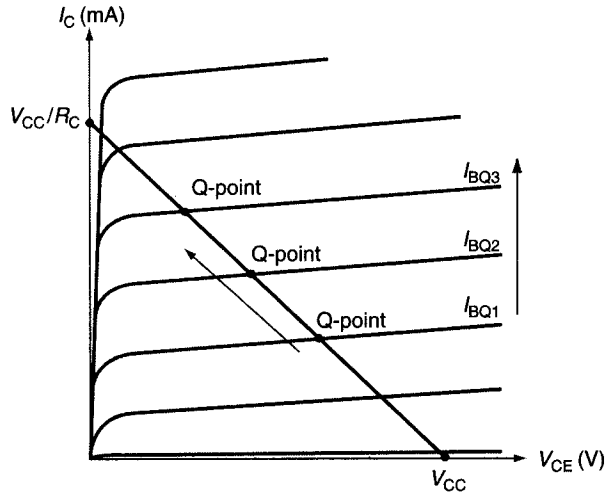


Figure 4.5 | Variation of operating point with base current.

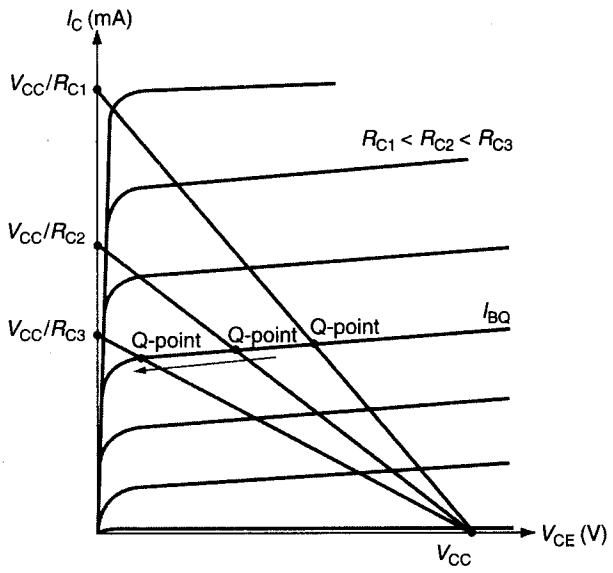


Figure 4.6 | Variation of operating point with collector resistor.

R_B. If the supply voltage (V_{CC}) is held constant and the value of the collector resistor (R_C) is changed, then the load line shifts as shown in Figure 4.6. Therefore, the operating point also shifts for the same value of base current (I_B) as shown in the figure. The variation of the load line and the operating point due to change in the supply voltage (V_{CC}) is illustrated in Figure 4.7.

The circuit shown employs NPN transistor and the network equations have been derived for NPN transistors. Same analysis applies to PNP transistors with the direction of currents and the polarities of the voltages reversed.

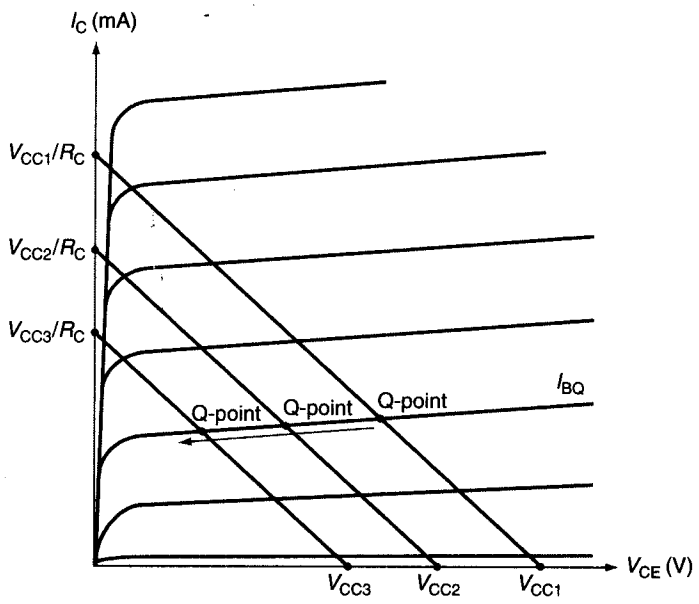


Figure 4.7 | Variation of operating point with supply voltage.

Advantages and Disadvantages

Fixed-bias circuit is the simplest possible biasing circuit requiring a very few components. However, the circuit offers worst stability against variations in temperature or transistor gain (β) as compared to the other configurations. It is therefore prone to thermal runaway and is very rarely used.

EXAMPLE 4.1

For the fixed-bias circuit of Figure 4.8, determine the operating point (given that transistor gain $\beta = 100$, $V_{BE} = 0.7$ V). Also draw the load line for the circuit.

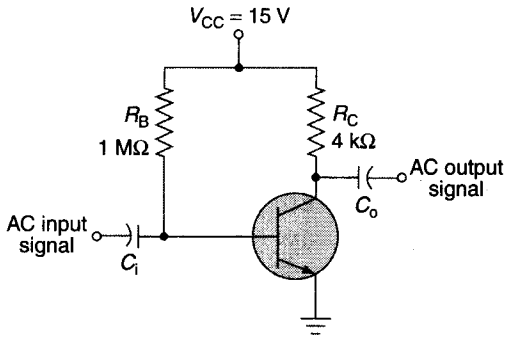


Figure 4.8 | Example 4.1.

Solution

1. The value of collector current (I_{CQ}) is given by

$$I_{CQ} = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right)$$

Substituting the values we get

$$I_{CQ} = 100 \times (15 - 0.7)/1 \times 10^6 = 1.43 \text{ mA}$$

2. The value of the collector–emitter voltage (V_{CEQ}) is given by

$$V_{CEQ} = V_{CC} - I_{CQ} R_C$$

That is

$$V_{CEQ} = 15 - 1.43 \times 10^{-3} \times 4 \times 10^3 = 15 - 5.72 = 9.28 \text{ V}$$

3. The load line equation for a fixed-bias circuit is given by

$$V_{CE} = V_{CC} - I_C R_C$$

4. Substituting $I_C = 0$, $V_{CE} = V_{CC} = 15$ V, the coordinates of the load line on the X-axis are obtained as (0 mA, 15 V).
5. Substituting $V_{CE} = 0$, $I_C = V_{CC}/R_C = 15/4 \times 10^3 = 3.75$ mA, the coordinates of the load line on the Y-axis are obtained as (3.75 mA, 0 V).
6. Joining the two points we get the load line as shown in Figure 4.9.

Answer: The operating point is $I_{CQ} = 1.43$ mA and $V_{CEQ} = 9.28$ V. The load line is shown in Figure 4.9.

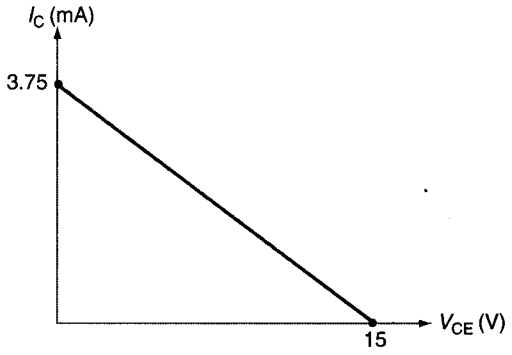


Figure 4.9 | Solution to Example 4.1.

Emitter-Bias or Self-Bias Configuration

Emitter-bias configuration, also referred to as self-bias configuration, has an additional emitter resistor (R_E) between the emitter terminal and ground as compared to the fixed-bias circuit (Figure 4.10). The addition of the resistor R_E provides improved stabilization as it introduces negative feedback into the circuit. The feedback type is current-series feedback as a voltage proportional to the output current is fed-back in series to the input.

DC Analysis

The DC equivalent of the emitter-bias circuit of Figure 4.10 is shown in Figure 4.11. The DC analysis is done on similar lines as that done for the fixed-bias circuit. Applying Kirchhoff's voltage law to the base–emitter loop we get

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

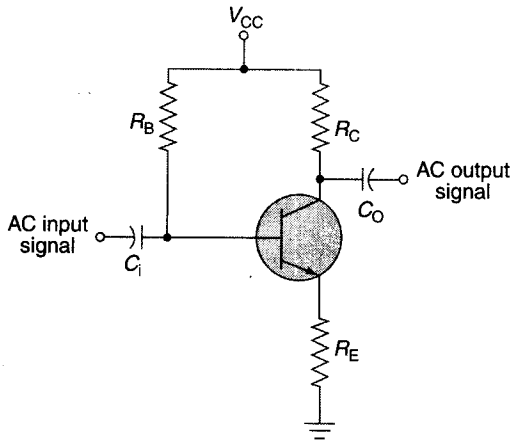


Figure 4.10 | Emitter-bias or self-bias circuit.

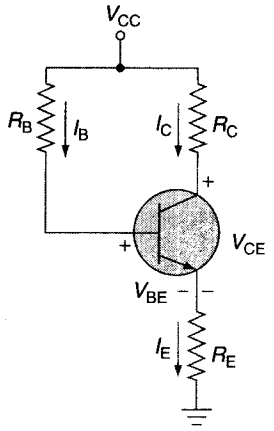


Figure 4.11 | DC equivalent of the emitter-bias circuit.

Substituting the value of emitter current (I_E) as $I_E = (\beta + 1)I_B$ in the above equation and rearranging the terms, the expression for I_B can be written as

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} \tag{4.10}$$

Voltage V_{BE} is small as compared to V_{CC} and can therefore be neglected. The expression for base current (I_B) is then given by

$$I_B \cong \frac{V_{CC}}{R_B + (\beta + 1)R_E} \tag{4.11}$$

From Eq. (4.10) we can infer that the emitter resistor (R_E) is reflected into the input circuit as $(\beta + 1)R_E$. In other words, R_E which is a part of the collector–emitter loop appears as $(\beta + 1)R_E$ in the

base–emitter loop. The fixed-bias circuit will have the same value of base current (I_B) when it has a base resistor equal to $[R_B + (\beta + 1)R_E]$. Therefore, the value of the input resistance for the emitter-bias circuit is given by

$$\text{Input resistance} = R_B + (\beta + 1)R_E \tag{4.12}$$

Applying Kirchhoff's voltage law to the collector–emitter loop, we get

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

Rearranging the terms of the equation we get the expression for the collector–emitter voltage (V_{CE}) as

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

As the emitter current (I_E) is approximately equal to the collector current (I_C), therefore

$$V_{CE} \cong V_{CC} - I_C(R_C + R_E) \tag{4.13}$$

The voltage of the emitter terminal of the transistor (V_E) is given by

$$V_E = I_E R_E \cong I_C R_E \tag{4.14}$$

The Q-point for the emitter-bias circuit is given by

$$I_{CQ} = \beta\left(\frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}\right), \quad V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E) \tag{4.15}$$

The emitter-bias circuit offers stability against variations in collector current due to change in temperature or change in the transistor gain (β). When the collector current increases, the emitter voltage increases. This results in decrease in the base–emitter potential which further leads to decrease in the value of base current. Therefore, the collector current also decreases, thereby compensating for the initial increase in its value.

Load-Line Analysis

The load-line analysis of the emitter-bias network differs slightly from that of the fixed-bias configuration. The load line in this configuration is given by

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \tag{4.16}$$

To draw the load line, substitute $I_C = 0$ in Eq. (4.16) following which we get

$$V_{CE} = V_{CC}\Big|_{I_C = 0}$$

This point appears on the horizontal axis (0, V_{CC}) of the output characteristics. Substituting $V_{CE} = 0$ in Eq. (4.16), we obtain I_C as

$$I_C = \frac{V_{CC}}{(R_C + R_E)}\Big|_{V_{CE} = 0}$$

This point appears on the vertical axis ($V_{CC}/(R_C + R_E)$, 0) of the output characteristics. The load line is obtained by joining these two points as shown in Figure 4.12. The operating point is established on the load line by determining the level of I_B using Eq. (4.10) or Eq. (4.11).

Advantages and Disadvantages

The emitter-bias circuit offers better stability than the fixed-bias circuit. However, maximum stability is offered by the circuit when the ratio of the base resistor (R_B) to the emitter resistor (R_E), that is R_B/R_E, is as

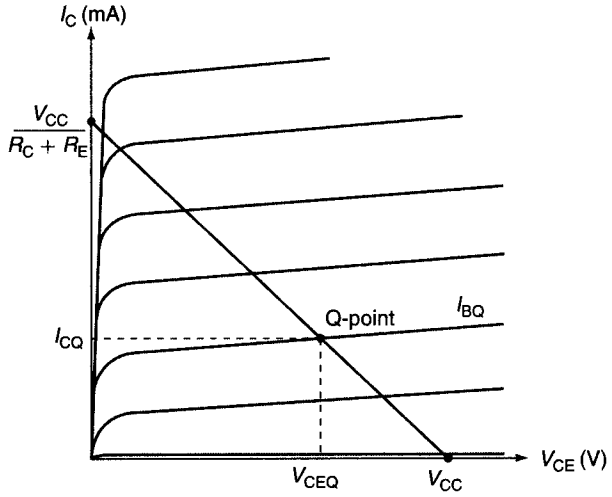


Figure 4.12 | Load-line analysis of the emitter-bias circuit.

small as possible. Thus, R_E should have a large value or R_B should be small. For large values of resistor R_E, larger collector supply voltage (V_{CC}) is needed. Also increase in R_E increases the negative feedback and reduces the gain of the circuit. For small values of resistor R_B, a separate base supply voltage is needed which adds to circuit complexity and is often not feasible. The disadvantages of the emitter-bias circuit are removed in the voltage-divider-bias with emitter-bias circuit.

EXAMPLE 4.2

Refer to Figure 4.13. Find the values of resistors R_B, R_C and R_E and the transistor gain β, given that $I_B = 40\ \mu A$, $I_C = 4\ mA$, $V_E = 2\ V$, $V_{CE} = 12\ V$ and supply voltage $V_{CC} = 15\ V$. Assume that the transistor used in the circuit is a silicon transistor.

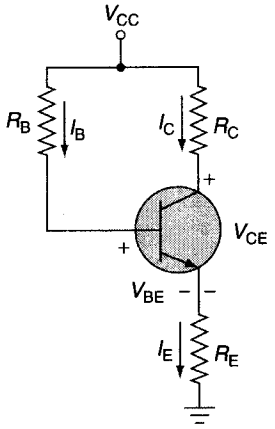


Figure 4.13 | Example 4.2.

Solution

1. $V_E = I_E R_E \cong I_C R_E$. Therefore

$$R_E = V_E / I_C = 2/4 \times 10^{-3} = 0.5\ \text{k}\Omega$$

2. $I_C = \beta I_B$. Therefore,

$$\beta = I_C / I_B = (4 \times 10^{-3})/(40 \times 10^{-6}) = 100$$

3. $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$40 \times 10^{-6} = \frac{15 - 0.7}{R_B + 101 \times 0.5 \times 10^3}$$

$$40 \times 10^{-6} \times (R_B + 50.5 \times 10^3) = 14.3$$

$$40 \times 10^{-6} \times R_B = 14.3 - 2.02 = 12.28$$

Therefore, $R_B = 307\ \text{k}\Omega$.

4. $V_{CE} = V_{CC} - I_C(R_C + R_E)$

$$12 = 15 - 4 \times 10^{-3} \times (R_C + 0.5 \times 10^3)$$

$$4 \times 10^{-3} \times R_C = 15 - 12 - 2 = 1$$

Therefore, $R_C = 0.25\ \text{k}\Omega$.

Answer: $R_E = 0.5\ \text{k}\Omega$, $R_B = 307\ \text{k}\Omega$, $R_C = 0.25\ \text{k}\Omega$, $\beta = 100$.

EXAMPLE 4.3

For the circuit shown in Figure 4.14, $V_{CC} = 15$ V, $V_{EE} = -10$ V, $R_C = 2$ kΩ, $R_E = 5$ kΩ, $R_B = 400$ kΩ and $\beta = 60$. Find the value of collector current (I_C) and the collector-to-emitter voltage (V_{CE}).

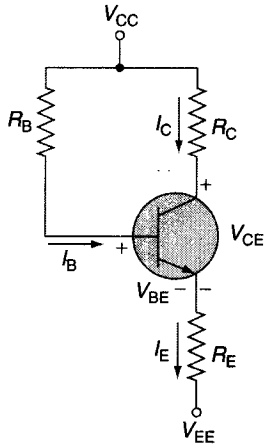


Figure 4.14 | Example 4.3.

Solution

1. Applying Kirchhoff's voltage law to the base–emitter loop of the circuit in Figure 4.14, we get

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E - V_{EE} = 0$$

2. Substituting $I_E = (\beta + 1)I_B$ in the above equation, we obtain the expression for I_B as

$$I_B = \frac{V_{CC} - V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$I_B = \frac{15 + 10 - 0.7}{400 \times 10^3 + 61 \times 5 \times 10^3}$$

$$= 24.3/(705 \times 10^3) = 34.46\ \mu A$$

3. $I_C = \beta I_B$. Therefore, $I_C = 60 \times 34.46 \times 10^{-6}$ A = 2.07 mA.
4. Applying Kirchhoff's law to the collector–emitter loop of the circuit in Figure 4.14, we get

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E - V_{EE} = 0$$

As $I_C \cong I_E$, therefore $V_{CE} = V_{CC} - V_{EE} - I_C(R_C + R_E)$.

5. $V_{CE} = 15 + 10 - 2.07 \times 10^{-3} \times (2 \times 10^3 + 5 \times 10^3) = 25 - 14.49 = 10.51$ V.

Answer: $I_C = 2.07$ mA, $V_{CE} = 10.51$ V.

Voltage-Divider-Bias with Emitter-Bias Configuration

The stability of the emitter-bias configuration is further improved if its input side is modified as shown in Figure 4.15. The circuit configuration is referred to as voltage-divider-bias with emitter-bias or simply the voltage-divider-bias configuration. It is the most commonly used transistor-biasing configuration. The name

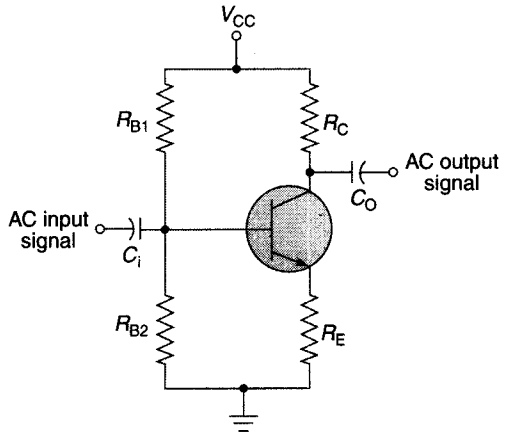


Figure 4.15 | Voltage-divider-bias with emitter-bias circuit.

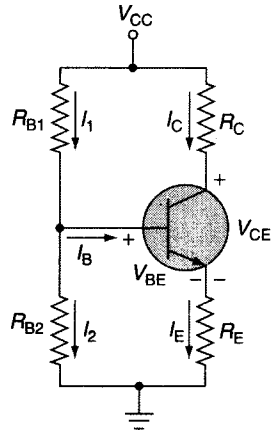


Figure 4.16 | DC equivalent of voltage-divider-bias circuit.

voltage-divider comes from the fact that the input section comprises a voltage divider of resistors R_{B1} and R_{B2} across the supply voltage V_{CC}. The circuit offers improved stability against variations in the temperature and the transistor gain.

DC Analysis

The DC equivalent of the voltage-divider-bias circuit of Figure 4.15 is shown in Figure 4.16. The circuit can be analyzed using two methods, namely, the accurate method and the approximate method. The accurate method is applicable to all circuits whereas the approximate method can be applied if certain conditions are met. We will discuss both the methods in subsequent paragraphs.

Accurate Method: Accurate method makes use of Thevenin's equivalent model of the input section. The input section of the circuit can be redrawn as shown in Figure 4.17(a) and can be simplified using Thevenin's equivalent theorem. Figure 4.17(b) shows the Thevenin's equivalent model. R_{TH} is the Thevenin's equivalent resistance and is determined by replacing the voltage source by a short circuit and calculating the resultant resistance of the circuit. R_{TH} is equal to the parallel combination of resistors R_{B1} and R_{B2} and is given by

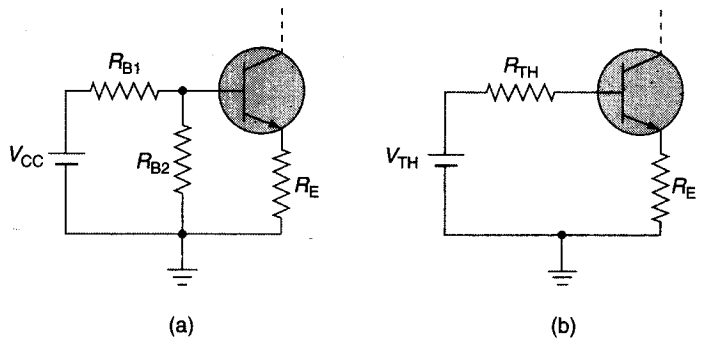


Figure 4.17 | (a) Input section of the voltage-divider-bias configuration; (b) Thevenin's equivalent of the input section of voltage-divider-bias configuration.

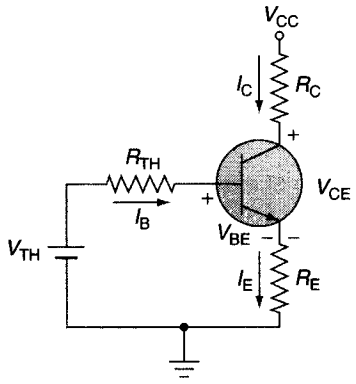


Figure 4.18 | Thevenin's equivalent of voltage-divider-bias configuration.

$$R_{TH} = R_{B1} \| R_{B2} = \frac{R_{B1} R_{B2}}{R_{B1} + R_{B2}} \tag{4.17}$$

V_{TH} is the open-circuit Thevenin's voltage and is equal to the voltage drop across the resistor R_{B2}:

$$V_{TH} = \frac{R_{B2} V_{CC}}{R_{B1} + R_{B2}} \tag{4.18}$$

Figure 4.18 shows the complete circuit using Thevenin's equivalent model. Applying Kirchhoff's voltage law to the base–emitter loop of the circuit in Figure 4.18, we get

$$V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E = 0 \tag{4.19}$$

Substituting $I_E = (\beta + 1) I_B$, we get the expression for I_B as

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1) R_E} \tag{4.20}$$

The expression is similar to the one derived for emitter-bias configuration with the term R_B being replaced by R_{TH}. If the base–emitter voltage (V_{BE}) is small as compared to the Thevenin's voltage (V_{TH}), then Eq. (4.20) can be approximated as

$$I_B \cong \frac{V_{TH}}{R_{TH} + (\beta + 1) R_E} \tag{4.21}$$

After determining the base current (I_B), the collector–emitter voltage (V_{CE}) can be determined by applying Kirchhoff's voltage law to the collector–emitter loop,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

As $I_C \cong I_E$, the value of collector–emitter voltage (V_{CE}) is given by

$$V_{CE} \cong V_{CC} - I_C (R_C + R_E) \tag{4.22}$$

The operating point is given by

$$I_{CQ} = \beta \left(\frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1) R_E} \right), \quad V_{CEQ} = V_{CC} - I_{CQ} (R_C + R_E) \tag{4.23}$$

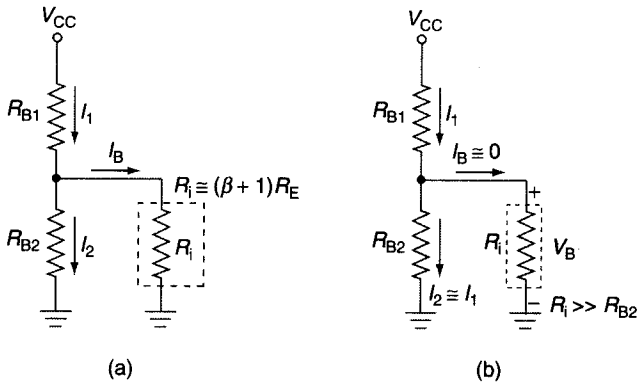


Figure 4.19 | Approximate method for analysis of voltage-divider-bias configuration.

Approximate Method: The input section of the voltage-divider with emitter-bias configuration can be redrawn as shown in Figure 4.19(a). The resistance R_i is the equivalent resistance between the base terminal and the ground and is referred to as the input resistance. Its value is given by

$$R_i \cong (\beta+1)R_E \tag{4.24}$$

If the value of resistance R_i is much larger than the resistance R_{B2}, then the base current (I_B) will be much smaller than the current I_2 and can be neglected. In that case it is assumed that the base current I_B is equal to zero and current I_1 is equal to current I_2 [Figure 4.19(b)]. Therefore, resistors R_{B1} and R_{B2} can be considered as series elements and the voltage at the base terminal (V_B) is given by

$$V_B = \frac{R_{B2}V_{CC}}{R_{B1}+R_{B2}} \tag{4.25}$$

The emitter voltage (V_E) is expressed as

$$V_E = V_B - V_{BE} \tag{4.26}$$

and the emitter current (I_E) is given by

$$I_E = \frac{V_E}{R_E} \tag{4.27}$$

As collector current (I_C) and emitter current (I_E) are approximately equal, the value of I_C is

$$I_C \cong \frac{V_E}{R_E} \tag{4.28}$$

The collector–emitter voltage (V_{CE}) is given by

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \tag{4.29}$$

It may be mentioned here that the approximate method can be applied if the value of the input resistance R_i is equal to greater than 10 times the resistance R_{B2}. That is

$$(\beta+1)R_E \geq 10R_{B2} \tag{4.30}$$

Load-line Analysis: The output circuit of the voltage-divider-bias configuration is the same as that of the emitter-bias configuration. This results in the same load line for the two configurations. The level of base current (I_B) is however determined by a different equation in this case.

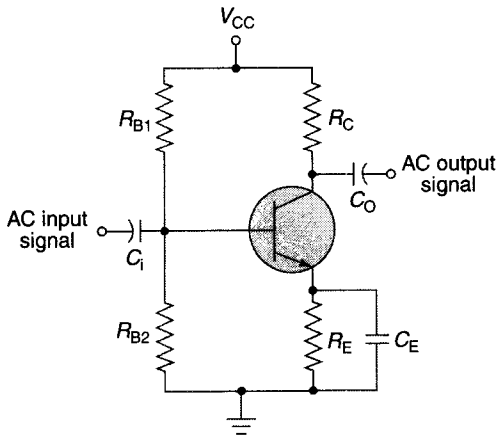


Figure 4.20 | Voltage-divider-bias configuration with emitter capacitor.

Advantages and Disadvantages

Voltage-divider-bias configuration is the most commonly used configuration as it provides excellent stabilization against variations in temperature and transistor gain (β). This is because the emitter resistor introduces negative feedback in the circuit. But negative feedback results in reduction of AC gain of the circuit. This problem can be solved by using a capacitor C_E in parallel with resistor R_E (Figure 4.20). The capacitor does not affect the DC analysis as it acts as an open circuit for DC voltages. For AC inputs, it acts as a short circuit, making the voltage across the emitter resistor (R_E) equal to zero and thus removing the problem of AC negative feedback.

EXAMPLE 4.4 *Determine the values of the resistors R_C and R_E for the circuit in Figure 4.21 given that $R_1 = 5\ k\Omega$, $R_2 = 1\ k\Omega$, $\beta = 200$, $V_{BE} = 0.7\ V$, $I_1 >> I_B$, $V_{CEQ} = 5\ V$ and $I_{CQ} = 2\ mA$.*

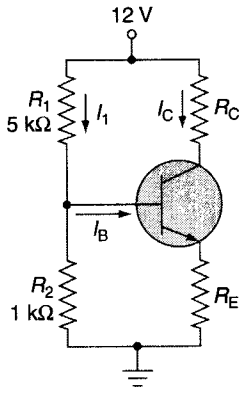


Figure 4.21 | Example 4.4.

Solution

1. Applying Kirchhoff's voltage loop to the collector–emitter loop of the circuit, we get

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

2. Assuming that $I_C \cong I_E$ and substituting the values in the above equation, we get

$$12 - 2\times10^{-3} \times R_C - 5 - 2\times10^{-3} \times R_E = 0$$

Therefore, $R_C + R_E = 3.5$ kΩ.

3. It is given that current I_1 is much greater that the base current I_B. Therefore, the approximate method can be used to analyze the circuit. The base voltage (V_B) is given by $V_B = 12 \times R_2/(R_1 + R_2) = 12 \times 1 \times 10^3/(5 \times 10^3 + 1 \times 10^3) = 2$ V.
4. The emitter voltage (V_E) is given by $V_E = V_B - V_{BE}$. As $V_{BE} = 0.7$ V, therefore $V_E = (2 - 0.7)$ V = 1.3 V.
5. $V_E = I_E R_E$. Therefore, $R_E = 1.3/2 \times 10^{-3} = 0.65$ kΩ.
6. Also as $R_C + R_E = 3.5$ kΩ, therefore, $R_C = (3.5 - 0.65)$ kΩ = 2.85 kΩ.

Answer: The values of resistors R_C and R_E are 2.85 kΩ and 0.65 kΩ, respectively.

EXAMPLE 4.5

For the circuit in Figure 4.22, determine the output voltage of the circuit when the adjust terminal of the potentiometer is at

(a) full-down position (position C);
(b) middle position (position B);
(c) top-most position (position A).

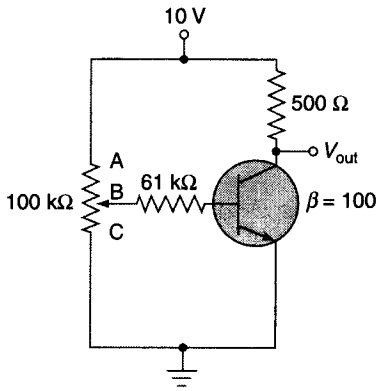


Figure 4.22 | Example 4.5.

Solution

(a) Potentiometer in full-down position (position C)

1. Figure 4.23(a) shows the circuit. Both the base and the emitter voltages are zero. Therefore $V_{BE} = 0$. Hence, the transistor is not conducting.
2. As a result, the output voltage is equal to the supply voltage, that is 10 V.

(b) Potentiometer in the middle position (position B)

1. Figure 4.23(b) shows the circuit. Applying Thevenin's theorem to the input section of the circuit in Figure 4.23(b), Thevenin's equivalent resistance (R_{TH}) is: $R_{TH} = (50 \times 10^3 \times 50 \times 10^3)/(50 \times 10^3 + 50 \times 10^3) = 25$ kΩ.
2. The open-circuit Thevenin's equivalent voltage (V_{TH}) is given by

$$V_{TH} = (10 \times 50 \times 10^3)/(50 \times 10^3 + 50 \times 10^3) = 5 \text{ V}$$

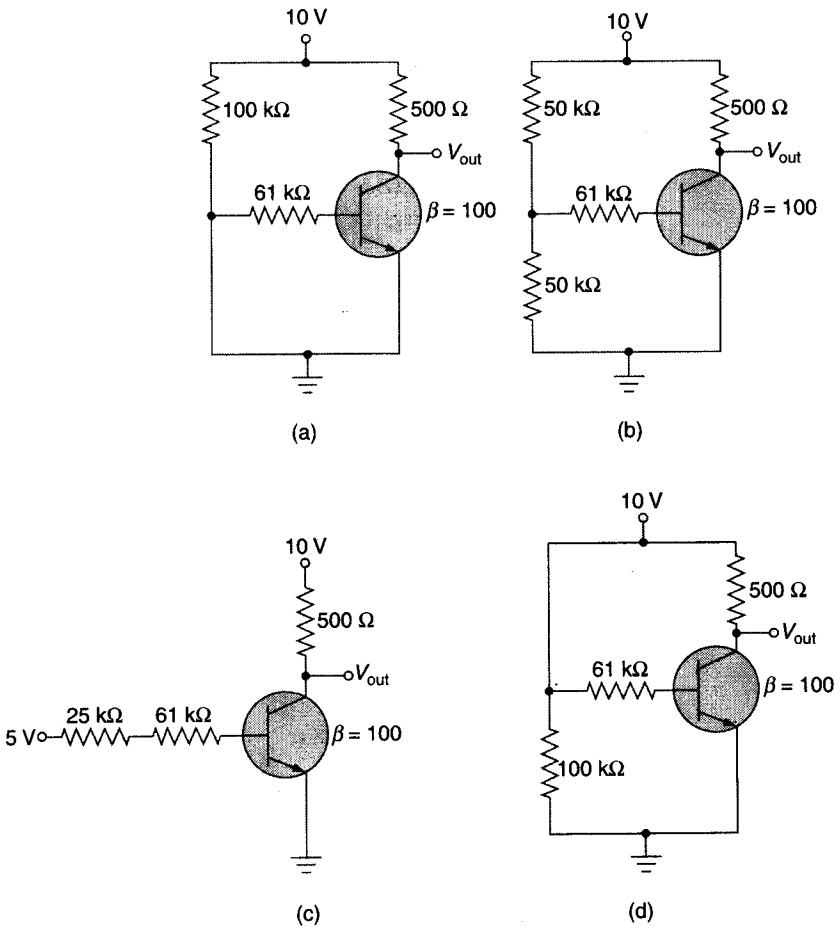


Figure 4.23 (a) Solution to part (a) Example 4.5; (b) and (c) solution to part (b) Example 4.5; (d) solution to part (c) Example 4.5.

3. The simplified circuit is shown in Figure 4.23(c).
4. Applying Kirchhoff's voltage law to the input circuit, we get
$$5 - 25 \times 10^3 \times I_B - 61 \times 10^3 \times I_B - 0.7 = 0$$
5. Therefore, $I_B = (4.3/86) \times 10^{-3}$ A = 50 μA.
6. $I_C = \beta \times I_B$. Therefore, $I_C = 100 \times 50 \times 10^{-6} = 5$ mA.
7. Applying Kirchhoff's voltage law to the output section of the circuit and solving for output voltage (V_{out}) we get
$$V_{out} = 10 - 0.5 \times 10^3 \times 5 \times 10^{-3} = 7.5 \text{ V}$$

(c) Potentiometer in top-most position (position A)

1. Figure 4.23(d) shows the circuit when the adjust terminal of the potentiometer is at position A.

2. Applying Kirchhoff's voltage law to the input section we get

$$10 - 61\times10^{3}\times I_B - 0.7 = 0$$

$$I_B = (9.3/61)\times10^{-3}\ \text{A} = 152\ \mu\text{A}$$

3. $I_E \cong I_C = \beta \times I_B = 100 \times 152 \times 10^{-6}\ \text{A} = 15.2\ \text{mA}$.
4. Applying Kirchhoff's voltage law to the output section and solving for the output voltage (V_{out}) we get

$$V_{out} = 10 - 0.5\times10^{3}\times15.2\times10^{-3}$$

$$= 10 - 7.6 = 2.4\ \text{V}$$

Answer: (a) The output voltage is 10 V; (b) output voltage is 7.5 V; (c) output voltage is 2.4 V.

EXAMPLE 4.6

Draw the DC equivalent of the circuit shown in Figure 4.24. Calculate the quiescent value of emitter current (I_{EQ}) using both the approximate and the accurate method. What is the percentage error introduced using the approximate method, given that transistor gain β is 165?

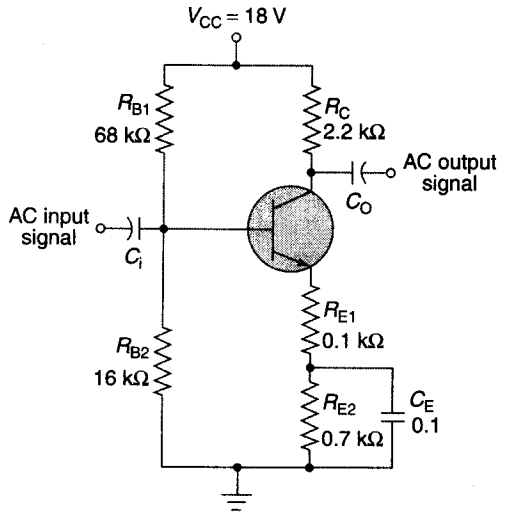


Figure 4.24 | Example 4.6.

Solution

1. The DC equivalent circuit is shown in Figure 4.25(a). The DC equivalent circuit is drawn by making all capacitors open and all the AC sources are considered to be zero. Resistor R_E is equal to the sum of the resistors R_{E1} and R_{E2}.

Using the Accurate Method

2. Applying Thevenin's theorem to the input section, the circuit reduces to the one shown in Figure 4.25(b).
3. The value of the Thevenin's equivalent resistance R_{TH} is 68 kΩ||16 kΩ = 12.95 kΩ.

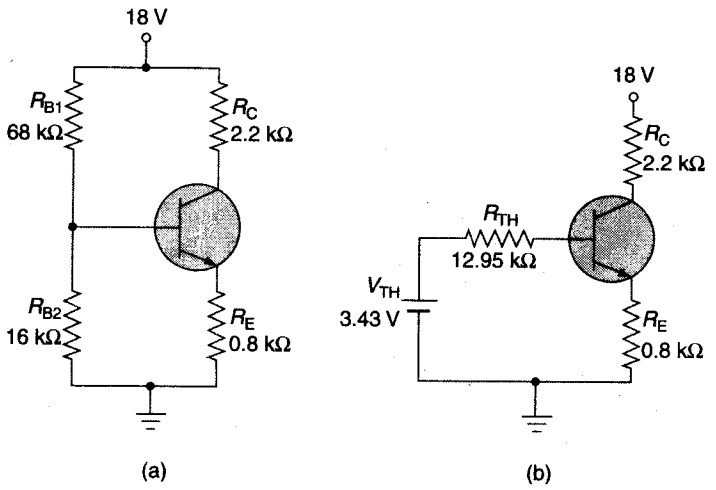


Figure 4.25 | Solution to Example 4.6.

4. The value of the Thevenin's equivalent voltage (V_{TH}) is

$$V_{TH} = (18 \times R_{B2})/(R_{B1} + R_{B2})$$
$$= (18 \times 16 \times 10^3)/(68 \times 10^3 + 16 \times 10^3)$$
$$= 3.43 \text{ V}$$

5. Applying Kirchhoff's voltage law to the emitter–base loop of the circuit in Figure 4.25(b), we get

$$3.43 - 12.95 \times 10^3 \times I_B - 0.7 - 0.8 \times 10^3 \times I_E = 0$$

6. Substituting $I_E = (\beta + 1)I_B = 166 \times I_B$ in the above equation, we obtain

$$2.73 - 12.95 \times 10^3 \times I_B - 132.8 \times 10^3 \times I_B = 0$$
$$I_B = 18.7 \mu\text{A}$$

7. $I_C = \beta I_B$. Therefore, $I_C = 165 \times 18.7 \times 10^{-6} = 3.08$ mA.

8. Applying Kirchhoff's voltage law to the collector–emitter loop of the circuit in Figure 4.25(b), we get

$$18 - 2.2 \times 10^3 \times I_C - V_{CE} - 0.8 \times 10^3 \times I_E = 0$$

Assuming, $I_C \cong I_E$ in the above equation, we get

$$V_{CE} = 18 - 3 \times 10^3 \times I_C = 18 - 3 \times 10^3 \times 3.08 \times 10^{-3} = 18 - 9.24 = 8.76 \text{ V}$$

Therefore, $V_{CE} = 8.76$ V.

9. The operating point as calculated using accurate method is ($I_C = 3.08$ mA, $V_{CE} = 8.76$ V).

Using the Approximate Method

10. The voltage at the base terminal (V_B) is

$$V_B = 18 \times R_{B2}/(R_{B1} + R_{B2}) = 18 \times 16 \times 10^3/(68 \times 10^3 + 16 \times 10^3) = 3.43 \text{ V}$$

11. Therefore, the voltage at the emitter terminal (V_E) is

$$V_E = V_B - V_{BE} = (3.43 - 07)\text{V} = 2.73 \text{ V}$$

12. $V_E = R_E \times I_E$, therefore the emitter current (I_E) is equal to
$$I_E = 2.73/0.8 \times 10^3 = 3.41 \text{ mA}$$
13. Applying Kirchhoff's voltage law to the collector–emitter loop, we get
$$18 - 2.2 \times 10^3 \times I_C - V_{CE} - 0.8 \times 10^3 \times I_E = 0$$
Assuming, $I_C \cong I_E$, in the above equation, we get
$$V_{CE} = 18 - 3 \times 10^3 \times 3.41 \times 10^{-3} = 7.77 \text{ V}$$
14. The operating point as calculated using the approximate method is (I_C = 3.41 mA, V_{CE} = 7.77 V).
15. The percentage error in the value of I_C using approximate method is
$$[(3.41 - 3.08)/3.08] \times 100\% = 10.71\%$$
16. The percentage error in the value of V_{CE} using the approximate method is
$$[(7.77 - 8.76)/8.76] \times 100\% = -11.3\%$$

Answer: Operating point using accurate method is (I_C = 3.08 mA, V_{CE} = 8.76 V).
Operating point using approximate method is (I_C = 3.41 mA, V_{CE} = 7.77 V).
Percentage error in I_C is 10.71% and in V_{CE} is −11.3%.

Collector-to-Base-Bias Configuration

In collector-to-base-bias configuration, the base-bias voltage is obtained from the collector of the transistor instead of the collector supply voltage (V_{CC}) as shown in Figure 4.26. This configuration is also referred to as feedback-bias configuration. The circuit offers better stability of the operating point against variations in temperature and transistor gain (β) due to negative feedback. The configuration has voltage-shunt feedback as the output voltage is fed-back in shunt to the input through base resistor (R_B).

DC Analysis

Figure 4.27 shows the DC equivalent of the collector-to-base-bias circuit in Figure 4.26. The current in the resistor R_C through supply voltage V_{CC} is split into two parts at the collector junction, one flowing into the collector terminal (I_C) and the other flowing through the base resistor (R_B). The current in resistor R_B is equal to the base current (I_B). Therefore, the current through resistor R_C is the sum of the base current (I_B) and the collector current (I_C).

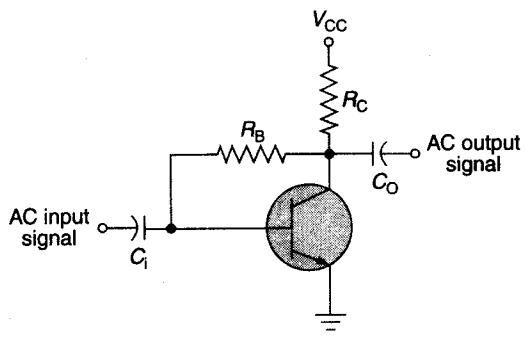


Figure 4.26 Collector-to-base-bias configuration.

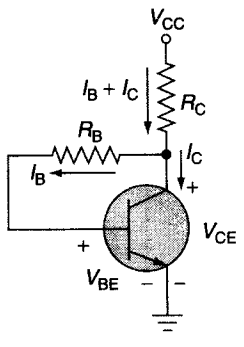


Figure 4.27 DC equivalent of collector-to-base-bias configuration.

Applying Kirchhoff's voltage law to the base–emitter loop of the circuit in Figure 4.27, we obtain

$$V_{CC} - (I_B + I_C)R_C - I_B R_B - V_{BE} = 0$$

Substituting $I_C = \beta I_B$ in the above equation and solving the equation for I_B we get

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_C} \tag{4.31}$$

This equation can be compared with that of emitter-bias configuration where the base current (I_B) was given by

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

The term R_E in the expression for base current (I_B) for emitter-bias configuration has been replaced by the term R_C in the collector-to-base-bias configuration.

The value of collector current (I_C) is given by $I_C = \beta I_B$. Therefore,

$$I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_C}\right) \tag{4.32}$$

As the value of β is very large, $(\beta + 1)$ can be approximated as β. Therefore, collector current (I_C) is equal to

$$I_C \cong \beta\left(\frac{V_{CC} - V_{BE}}{R_B + \beta R_C}\right)$$

If the value of βR_C is much greater than R_B, then the term $R_B + \beta R_C$ can be approximated as βR_C and in this case the value of collector current I_C is

$$I_C \cong \beta\left(\frac{V_{CC} - V_{BE}}{\beta R_C}\right) = \frac{V_{CC} - V_{BE}}{R_C}$$

Therefore, the collector current becomes independent of the value of transistor gain (β). In other words, the stability offered by the collector-to-base configuration improves as the value of the collector resistor (R_C) increases.

Applying Kirchhoff's voltage law to the collector–emitter loop, we get

$$V_{CC} - (I_B + I_C)R_C - V_{CE} = 0$$

Ignoring base current (I_B) because its value is negligible compared to the collector current (I_C), we get

$$V_{CE} \cong V_{CC} - I_C R_C \tag{4.33}$$

The value of the operating point for collector-to-base-bias configuration is given by

$$I_{CQ} = \beta\left(\frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_C}\right), V_{CEQ} = V_{CC} - I_{CQ}R_C \tag{4.34}$$

Load-line Analysis: The load-line analysis for collector-to-base-bias configuration can be carried on similar lines to that done in the case of emitter-bias configuration.

Another variation of the collector-to-base-bias circuit is to place an emitter resistor (R_E) between the emitter terminal of the transistor and the ground as shown in Figure 4.28. In that case, the equations for the base current (I_B), collector current (I_C) and the collector–emitter voltage (V_{CE}) are as follows:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)(R_C + R_E)} \tag{4.35}$$

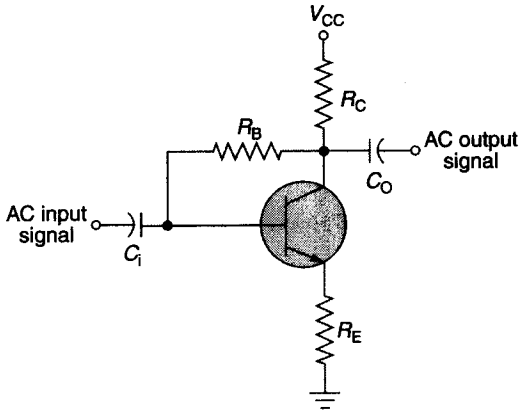


Figure 4.28 | Collector-to-base-bias configuration with emitter resistor.

$$I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B + (\beta+1)(R_C + R_E)}\right) \tag{4.36}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \tag{4.37}$$

The collector-to-base-bias configuration with emitter resistor offers better stability than emitter-bias configuration and collector-to-base-bias configuration without emitter resistor.

Advantages and Disadvantages

The collector-to-base-bias circuit provides stability to the operating point against variations in temperature and transistor gain (β). However, due to negative feedback, the AC voltage gain of the amplifier is reduced. This problem is partially solved by splitting the resistor R_B into two parts and by connecting a capacitor C_B as shown in Figure 4.29. For the AC signal, capacitor C_B acts as a short circuit and the effective base resistance R_B is reduced to half. This reduces the AC negative feedback and increases the AC voltage gain offered by the circuit.

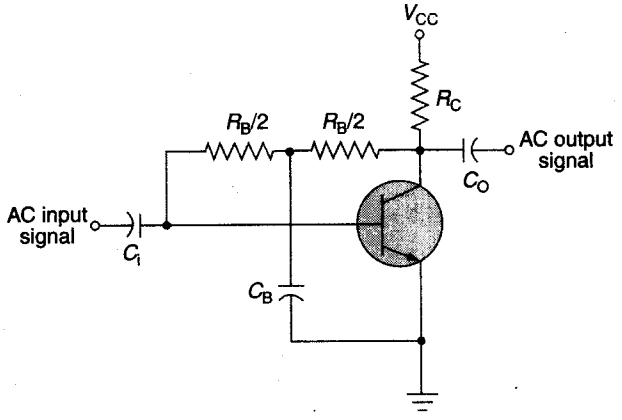


Figure 4.29 | Collector-to-base bias with capacitor to reduce AC negative feedback.

Also, the base resistor (R_B) in collector-to-base-bias configuration has a smaller value than that used in fixed-bias or the emitter-bias configurations. Therefore, in this case the base current changes more with temperature. Hence, the advantage of better stability factor offered by collector-to-base-bias configuration is offset by the larger variation in the base current.

EXAMPLE 4.7

Determine the operating point of the collector-to-base-bias circuit of Figure 4.30. The value of the transistor gain β is 100 and the base-emitter voltage (V_{BE}) of the transistor is 0.7 V. Also find the percentage change in the value of operating point when the value of β increases by 50%.

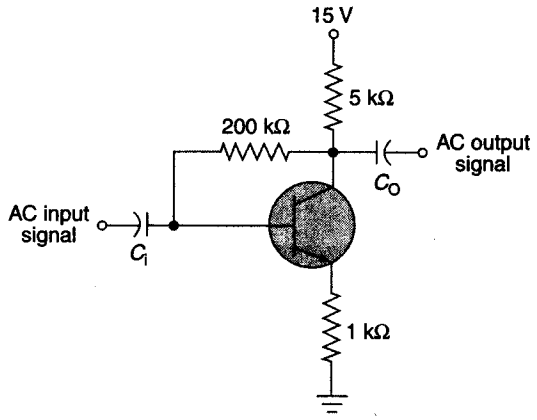


Figure 4.30 | Example 4.7.

Solution

1. The value of base current is

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)(R_C + R_E)}$$
$$= \frac{15 - 0.7}{200\times10^3 + 101\times(5\times10^3 + 1\times10^3)}$$
$$= \frac{14.3}{806\times10^3}$$
$$= 17.74\ \mu A$$

2. Collector current $I_C = \beta I_B = 100 \times 17.74 \times 10^{-6} = 1.77$ mA.
3. The value of collector–emitter voltage is

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 15 - 1.77\times10^{-3}\times(5\times10^3 + 1\times10^3)$$
$$= 15 - 10.62 = 4.38\ V$$

4. The operating point for $\beta = 100$ is (1.77 mA, 4.38 V).
5. When the value of β increases by 50%, value of new β is equal to 150.

6. The value of base current is

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)(R_C + R_E)}$$
$$= \frac{15 - 0.7}{200\times10^3 + 151\times(5\times10^3 + 1\times10^3)}$$
$$= \frac{14.3}{1106\times10^3}$$
$$= 12.93\ \mu A$$

7. Collector current $I_C = \beta I_B = 150 \times 12.93 \times 10^{-6} = 1.94$ mA.
8. The value of collector–emitter voltage is

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 15 - 1.94\times10^{-3} \times (5\times10^3 + 1\times10^3)$$
$$= 15 - 11.64 = 3.36\ V$$

9. The operating point for $\beta = 150$ is (1.94 mA, 3.36 V).
10. Percentage change in collector current = [(1.94–1.77)/1.77] × 100% = 9.6%.
11. Percentage change in collector–emitter voltage = [(3.36–4.38)/4.38] × 100% = –23.3%.

Answer: The operating point for $\beta = 100$ is (1.77 mA, 4.38 V).
The percentage change in collector current is 9.6% and in collector–emitter voltage is –23.3%.

4.3 Common-Base Circuit

In the common-base circuit, as we have studied in Chapter 3, the input is applied to the emitter terminal and the output is taken from the collector terminal. The base terminal is common to both the input and the output sections. Figure 4.31 shows the circuit for common-base configuration. The DC equivalent of the circuit is shown in Figure 4.32.

The analysis of the input section determines the emitter current (I_E). Applying Kirchhoff's voltage law to the input section (emitter–base loop), we get

$$V_{EE} - I_E R_E - V_{BE} = 0$$

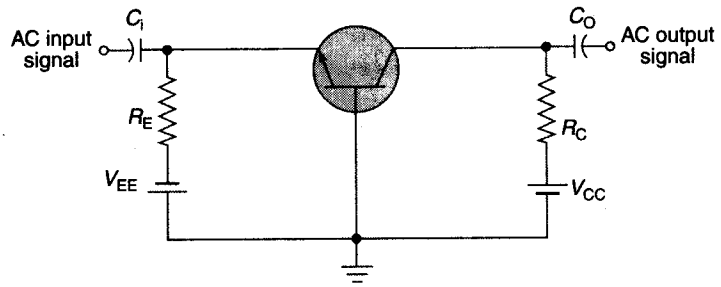


Figure 4.31 | Common-base circuit.

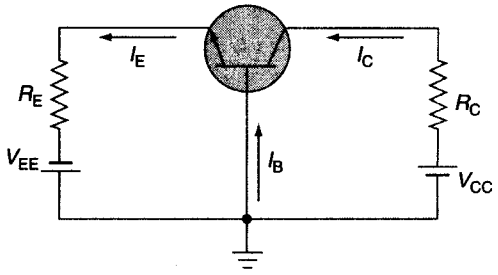


Figure 4.32 DC equivalent of common-base circuit.

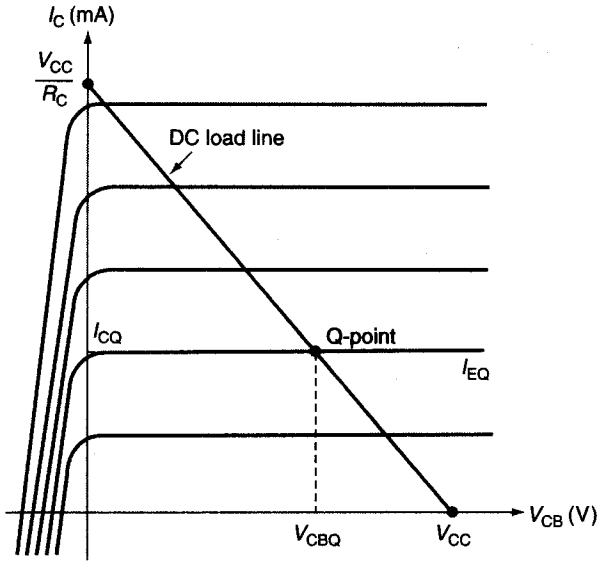


Figure 4.33 Load-line analysis of common-base configuration.

Therefore, the emitter current (I_E) is equal to

$$I_E = \frac{V_{EE} - V_{BE}}{R_E} \tag{4.38}$$

As the collector current (I_C) ≅ emitter current (I_E), the value of collector current (I_C) is also given by Eq. (4.38). Applying Kirchhoff's voltage law to the output section (collector–base loop), we get

$$V_{CC} - V_{CB} - I_C R_C = 0$$

Therefore,

$$V_{CB} = V_{CC} - I_C R_C \tag{4.39}$$

The operating point for the common-base configuration is given by

$$I_{CQ} = \frac{V_{EE} - V_{BE}}{R_E}, \quad V_{CBQ} = V_{CC} - I_{CQ} R_C \tag{4.40}$$

Load-line Analysis The load line is drawn using the output equation given by Eq. (4.39). Substituting $I_C = 0$ in Eq. (4.39), we get

$$V_{CB} = V_{CC}\big|_{I_C = 0}$$

Substituting $V_{CB} = 0$ in Eq. (4.39), we get

$$I_C = \frac{V_{CC}}{R_C}\bigg|_{V_{CB} = 0}$$

Joining the two points we can draw the DC load line on the output characteristics (Figure 4.33). The operating point (I_{CQ}, V_{CBQ}) is determined by the point of intersection of the load line with the characteristic curves at the quiescent value of emitter current given by Eq. (4.38).

EXAMPLE 4.8 *Determine the operating point for the circuit shown in Figure 4.34 given that the transistor base–emitter voltage (V_{BE}) is 0.7 V.*

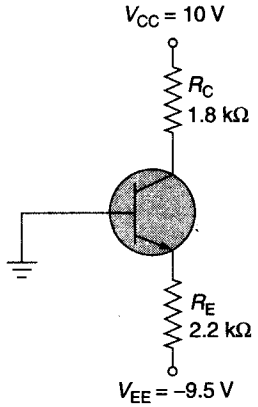


Figure 4.34 | Example 4.8.

Solution

1. The value of the emitter current is

$$I_E = \frac{-V_{EE} - V_{BE}}{R_E}$$

$$I_E = (9.5 - 0.7) / 2.2 \times 10^3 = 4 \text{ mA}$$

2. The value of collector current $I_C \cong I_E$. Therefore, $I_C = 4$ mA.

$$V_{CB} = V_{CC} - I_C R_C$$

3. The output voltage is given by $= 10 - 4 \times 10^{-3} \times 1.8 \times 10^3$.

$$= 10 - 7.2 = 2.8 \text{ V}$$

4. The operating point is $I_C = 4$ mA, $V_{CB} = 2.8$ V.

Answer: The operating point is $I_C = 4$ mA, $V_{CB} = 2.8$ V.

4.4 Common-Collector Circuit

In the common-collector configuration, also referred to as emitter-follower configuration, the input voltage is applied to the base terminal and the output is taken from the emitter terminal. The collector terminal is common to both the input and the output sections. Common-collector configuration exhibits 100% voltage-series feedback as whole of the output voltage is fed-back in series with the input voltage.

Figure 4.35 shows one of the possible circuits of common-collector configuration. The circuit is similar to that of voltage-divider bias with the difference that there is no collector resistor (R_C) and the output is taken from the emitter terminal instead of the collector terminal.

Figure 4.36(a) shows another possible common-collector circuit. Figure 4.36(b) shows the DC equivalent of the circuit. Applying Kirchhoff's voltage law to the base–emitter loop, we get

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

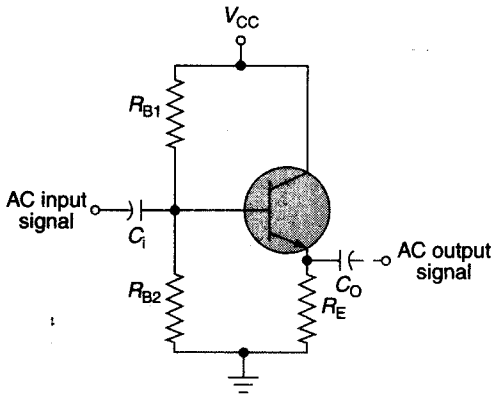


Figure 4.35 | One possible common-collector configuration.

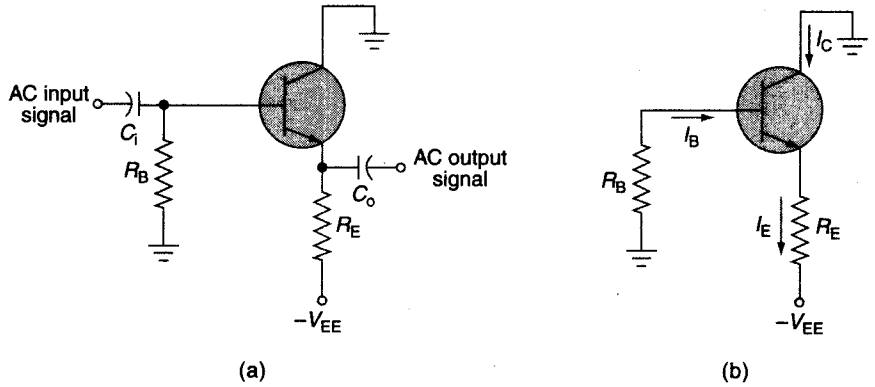


Figure 4.36 | (a) Another possible common-collector configuration; (b) DC equivalent of the circuit in part (a).

Substituting $I_E = (\beta + 1)I_B$ in the above equation and solving for base current (I_B), we get

$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E} \tag{4.41}$$

Applying Kirchhoff's voltage law to the emitter–collector loop, we get

$$-V_{EE} + I_E R_E + V_{CE} = 0$$

$$V_{CE} = V_{EE} - I_E R_E \tag{4.42}$$

Load-line analysis can be done on similar lines as for the common-emitter configuration.

EXAMPLE 4.9 | *Determine the output voltage (V_{out}) of the circuit shown in Figure 4.37 given that V_{BE} voltage for transistors Q_1 and Q_2 is 0.7 V.*

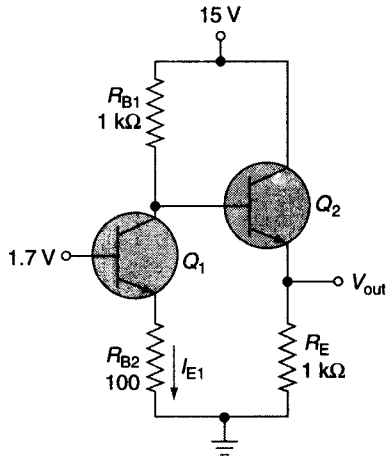


Figure 4.37 | Example 4.9.

Solution

1. Applying Kirchhoff's voltage law to the base–emitter loop of transistor Q_1, we get
$$1.7 - 0.7 - 100 \times I_{E1} = 0$$
$$I_{E1} = 10 \text{ mA}$$
2. Applying Kirchhoff's voltage law to the collector–emitter loop of transistor Q_1, we get
$$15 - 1 \times 10^3 \times I_{C1} - V_{C1} = 0$$
3. As $I_{E1} \cong I_{C1}$, therefore $V_{C1} = 15 - 1 \times 10^3 \times 10 \times 10^{-3} = 5$ V.
4. The base voltage of the transistor Q_2 = Collector voltage of transistor Q_1.
5. Therefore, base voltage of the transistor $Q_2 = 5$ V.
6. Emitter voltage of transistor Q_2 is given by $V_{E2} = V_{B2} - V_{BE2} = 5 - 0.7 = 4.3$ V.
7. Therefore, output voltage $V_{out} = V_{E2} = 4.3$ V.

Answer: The output voltage V_{out} is 4.3 V.

4.5 Bias Stabilization

Bias stabilization refers to the ability of a bias circuit to maintain a fixed operating point against variations in temperature and transistor gain (β). Bias stabilization is important as the transistor parameters are strongly dependent on temperature. The transistor gain (β) increases with increase in temperature, the base–emitter voltage (V_{BE}) of the transistor decreases with increase in temperature at a rate of 2.5 mV/°C for constant collector current and the leakage current (I_{CO}) doubles itself for every 10°C rise in temperature. As the base current (I_B) depends on V_{BE}, therefore it also varies with temperature. Collector current (I_C) is given by the expression $I_C = \beta I_B + (\beta + 1)I_{CO}$. Therefore, it varies with change in temperature as all the three parameters in its expression (β, I_B and I_{CO}) are temperature-dependent.

Figure 4.38 shows the typical output characteristics of a common–emitter transistor at two different temperatures. As it is evident from the figure, the CE output characteristics shift upwards with increase in

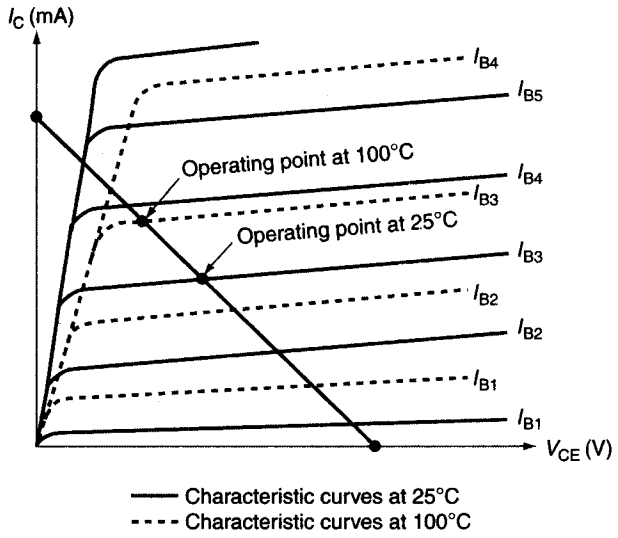


Figure 4.38 | Variation in the output characteristics of a transistor with change in temperature.

temperature as the leakage current (I_{CO}) increases with increase in temperature. The spacing between the adjacent curves also increases as the gain (β) of the transistor increases. Thus for the same base current, the operating point shifts and it may be possible that the transistor biased in the active region at one temperature finds itself in the saturation region at an elevated temperature.

Another important cause of variation in collector current (I_C) is the widespread variation in the value of transistor gain (β) of the order of three times for two transistors of the same type number. Thus for the same base current, the collector current varies with change in the transistor used in the circuit. Each of the biasing circuit described in preceding sections offers different amount of stability to the operating point. The amount of stability offered by the circuit is measured in terms of stability factor.

Stability Factor

Stability factor defines the extent to which the collector current (I_C) of a transistor is stable against variations in the transistor parameters, namely, the leakage current (I_{CO}), the transistor gain (β) and the base–emitter voltage (V_{BE}). The three types of stability factors are defined with respect to transistors, namely, $S_{I_{CO}}$, S_β and $S_{V_{BE}}$. Small value of stability factor indicates good bias stability whereas large value of stability factor indicates poor bias stability. Ideal value of stability factor is zero.

$S_{I_{CO}}$ is defined as the ratio of the change in the collector current (ΔI_C) with respect to change in the leakage current (ΔI_{CO}) with the base–emitter voltage (V_{BE}) and the transistor gain (β) held constant. It can be expressed mathematically as

$$S_{I_{CO}} = \left.\frac{\Delta I_C}{\Delta I_{CO}}\right|_{V_{BE}=\text{const.},\,\beta=\text{const.}} \tag{4.43}$$

$S_{V_{BE}}$ is defined as the ratio of change in the collector current (ΔI_C) with respect to change in the base–emitter voltage (ΔV_{BE}) with both the leakage current (I_{CO}) and the transistor gain (β) held constant:

$$S_{V_{BE}} = \left.\frac{\Delta I_C}{\Delta V_{BE}}\right|_{I_{CO}=\text{const.},\,\beta=\text{const.}} \tag{4.44}$$

S_β is defined as the ratio of the change in the collector current (ΔI_C) with respect to change in the transistor gain (β) keeping both the leakage current (I_{CO}) and the base–emitter voltage (V_{BE}) as constant:

$$S_\beta = \left.\frac{\Delta I_C}{\Delta \beta}\right|_{I_{CO}=\text{const.},\ V_{BE}=\text{const.}} \tag{4.45}$$

The total change in the collector current (ΔI_C) due to changes in the leakage current (ΔI_{CO}), the transistor gain ($\Delta\beta$) and the base–emitter voltage (ΔV_{BE}) is given by

$$\Delta I_C = S_{I_{CO}} \Delta I_{CO} + S_\beta \Delta\beta + S_{V_{BE}} \Delta V_{BE} \tag{4.46}$$

Stability Factor ($S_{I_{CO}}$)

In the following paragraphs, we will determine the value of stability factor ($S_{I_{CO}}$) offered by different biasing circuits.

Fixed-Bias Configuration

The collector current (I_C) is expressed in terms of the base current (I_B) as

$$I_C = \beta I_B + (\beta+1) I_{CO}$$

Differentiating collector current (I_C) with respect to the leakage current (I_{CO}) and keeping the transistor gain (β) and the base–emitter voltage (V_{BE}) as constant, we get

$$\frac{dI_C}{dI_{CO}} = (\beta+1)$$

The stability factor $S_{I_{CO}}$ for a fixed-bias circuit is given by

$$S_{I_{CO}} = \beta + 1 \tag{4.47}$$

If $\beta = 100$, then $S_{I_{CO}} = 101$, which implies that the collector current increases by 101 times than the increase in the leakage current. Therefore, for fixed-bias circuit the collector current (I_C) is strongly dependent on the change in the leakage current (I_{CO}) and hence on the temperature. In other words, fixed-bias circuit offers very poor stability against variations in the leakage current.

Emitter-Bias Configuration

As derived in Section 4.1, the voltage-current equation for the base–emitter loop of the emitter-bias configuration is given by

$$V_{CC} - V_{BE} - I_E R_E - I_B R_B = 0 \tag{4.48}$$

Substituting $I_E = I_B + I_C$ in Eq. (4.48) and rearranging the terms, we get

$$(R_B + R_E) I_B = V_{CC} - V_{BE} - I_C R_E$$

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_E}{R_B + R_E} \tag{4.49}$$

As $V_{BE} << V_{CC}$, Eq. (4.49) can be rewritten as

$$I_B = \frac{V_{CC} - I_C R_E}{R_B + R_E} \tag{4.50}$$

The collector current (I_C) is expressed as

$$I_C = \beta I_B + (\beta+1) I_{CO} \tag{4.51}$$

Substituting the value of I_B given by Eq. (4.50) in Eq. (4.51) we get

$$I_C = \beta\frac{(V_{CC} - I_C R_E)}{R_B + R_E} + (\beta+1)I_{CO} \tag{4.52}$$

Rearranging the terms of Eq. (4.52) we get

$$\frac{(R_B + R_E + \beta R_E)I_C}{R_B + R_E} = \frac{\beta V_{CC}}{R_B + R_E} + (\beta+1)I_{CO}$$

$$I_C = \frac{\beta V_{CC}}{R_B + (\beta+1)R_E} + \frac{(\beta+1)(R_B + R_E)I_{CO}}{R_B + (\beta+1)R_E} \tag{4.53}$$

Differentiating I_C in Eq. (4.53) with respect to I_{CO} keeping β and V_{BE} constant we get

$$\frac{dI_C}{dI_{CO}} = \frac{(\beta+1)(R_B + R_E)}{R_B + (\beta+1)R_E} = \frac{(\beta+1)(1 + R_B/R_E)}{1 + \beta + R_B/R_E}$$

Therefore, the stability factor $S_{I_{CO}}$ for emitter-bias configuration is given as

$$S_{I_{CO}} = \frac{(\beta+1)(1 + R_B/R_E)}{1 + \beta + R_B/R_E} \tag{4.54}$$

For $R_B/R_E >> (\beta + 1)$, Eq. (4.54) becomes

$$S_{I_{CO}} \cong \beta + 1 \tag{4.55}$$

For the other extreme, when $R_B/R_E << 1$

$$S_{I_{CO}} \cong 1 \tag{4.56}$$

Thus the stability factor ($S_{I_{CO}}$) for an emitter-bias circuit varies from approximately 1 to ($\beta + 1$) as the ratio of base resistor (R_B) to emitter resistor (R_E) increases from a very small value to a very large value (Figure 4.39). As we know, the stability factor should be as small as possible, therefore the ratio R_B/R_E should be as small as possible. Thus, resistor R_E should be sufficiently large. Increase in the value of R_E increases the negative feedback factor and reduces the gain of the circuit. Therefore, a trade-off needs to be applied that satisfies both the stability and circuit gain criteria.

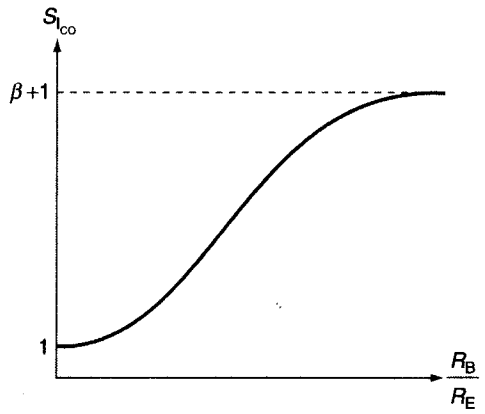


Figure 4.39 | Stability factor for emitter-bias circuit.

To sum up, the emitter-bias configuration offers some stability against variations in the leakage current I_{CO}. However, the stability offered is not very high as the ratio of R_B/R_E cannot be reduced beyond a certain value. This problem is overcome in the voltage-divider bias with emitter-bias configuration.

The fact that the emitter-bias configuration offers stability can also be explained logically, without going deep into mathematical calculations, with the help of the expression for the base current (I_B) for the configuration given as

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_E}{R_B + R_E} \tag{4.57}$$

When the value of collector current (I_C) increases due to increase in the leakage current (I_{CO}), the value of the base current (I_B) decreases, which in turn reduces the value of the collector current (I_C). This compensates for the initial increase in I_C. Thus, the circuit tries to maintain a constant collector current.

Voltage-Divider-Bias with Emitter-Bias Configuration

In the case of voltage-divider-bias configuration, the expression for $S_{I_{CO}}$ is similar to that of emitter-bias configuration, with the base resistor (R_B) being replaced by Thevenin's equivalent resistance (R_{TH}):

$$S_{I_{CO}} = \frac{(\beta+1)(1+R_{TH}/R_E)}{1+\beta+R_{TH}/R_E} \tag{4.58}$$

The circuit offers highest stability when the value of emitter resistor (R_E) is much larger than the Thevenin's equivalent resistance (R_{TH}). It must be remembered that in voltage-divider configuration, Thevenin's equivalent resistance (R_{TH}) is much smaller than the corresponding base resistor (R_B) of the emitter-bias configuration. Thus, the ratio R_E/R_{TH} is higher as compared to R_E/R_B in emitter-bias configuration. Hence, this configuration offers better stability as compared to the emitter-bias configuration.

Collector-to-Base-Bias Configuration

The expression for $S_{I_{CO}}$ for collector-to-base-bias configuration can be obtained in a manner similar to that for the emitter-bias configuration. The expression is given as

$$S_{I_{CO}} = \frac{(\beta+1)(1+R_B/R_C)}{1+\beta+R_B/R_C} \tag{4.59}$$

Hence, the ratio R_B/R_C should be as small as possible for better stability.

Stability Factor ($S_{V_{BE}}$)

$S_{V_{BE}}$ is defined as the ratio of change in the collector current (ΔI_C) with respect to change in the base–emitter voltage (ΔV_{BE}) with both the leakage current (I_{CO}) and the transistor gain (β) held constant. In the following sub-sections we derive the expression for $S_{V_{BE}}$ for different biasing circuits.

Fixed-Bias Circuit

The expression for collector current (I_C) is

$$I_C = \beta I_B + (\beta+1) I_{CO}$$

In the case of fixed-bias circuit, the expression for base current (I_B) is given by

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{4.60}$$

Substituting the value of base current (I_B) in the expression for collector current (I_C), we get

$$I_C = \frac{\beta(V_{CC} - V_{BE})}{R_B} + (\beta+1)I_{CO} \tag{4.61}$$

Differentiating Eq. (4.61) with respect to V_{BE} with I_{CO} and β constant, we get

$$\frac{dI_C}{dV_{BE}} = \frac{-\beta}{R_B}$$

Therefore, the stability factor $S_{V_{BE}}$ for a fixed-bias configuration is given by

$$S_{V_{BE}} = \frac{-\beta}{R_B} \tag{4.62}$$

As is clear from this equation, the stability factor ($S_{V_{BE}}$) of the fixed-bias circuit improves as the value of base resistor (R_B) increases.

Emitter-Bias Configuration

In the emitter-bias configuration the base current (I_B) is given by

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_E}{R_B + R_E} \tag{4.63}$$

The equation for collector current (I_C) is

$$I_C = \beta I_B + (\beta+1)I_{CO} \tag{4.64}$$

Substituting the value of base current (I_B) in Eq. (4.64), we get

$$I_C = \frac{\beta(V_{CC} - V_{BE} - I_C R_E)}{R_B + R_E} + (\beta+1)I_{CO} \tag{4.65}$$

Rearranging the terms in Eq. (4.65), we get

$$I_C = \frac{\beta(V_{CC} - V_{BE}) + (\beta+1)(R_B + R_E)I_{CO}}{R_B + (\beta+1)R_E} \tag{4.66}$$

Differentiating I_C in Eq. (4.66) with respect to V_{BE} keeping β and I_{CO} constant, we get

$$\frac{dI_C}{dV_{BE}} = \frac{-\beta}{R_B + (\beta+1)R_E} = \frac{-\beta/R_E}{R_B/R_E + (\beta+1)}$$

Thus the stability factor $S_{V_{BE}}$ for the emitter-bias configuration is given by

$$S_{V_{BE}} = \frac{-\beta/R_E}{R_B/R_E + (\beta+1)} \tag{4.67}$$

When $(\beta + 1) >> R_B/R_E$, the value of stability factor is given by

$$S_{V_{BE}} = \frac{-\beta/R_E}{\beta+1} \cong \frac{-1}{R_E} \tag{4.68}$$

We can see from Eq. (4.68) the stability of the emitter–bias circuit against variations in base–emitter voltage (V_{BE}) improves with increase in the value of emitter resistance (R_E).

Voltage-Divider Bias with Emitter-Bias Configuration

In the case of voltage-divider-bias configuration, the expression for $S_{V_{BE}}$ is similar to that of emitter-bias configuration with the base resistor (R_B) replaced by Thevenin's equivalent resistance (R_{TH}):

$$S_{V_{BE}} = \frac{-\beta / R_E}{R_{TH}/R_E + (\beta + 1)} \tag{4.69}$$

Collector-to-Base-Bias Configuration

In the case of collector-to-base-bias configuration, the expression for $S_{V_{BE}}$ is similar to that of emitter-bias configuration except that the emitter resistor (R_E) is replaced by collector resistor (R_C):

$$S_{V_{BE}} = \frac{-\beta / R_C}{R_B/R_C + (\beta + 1)} \tag{4.70}$$

Stability Factor (S_β)

S_β is defined as the ratio of the change in the collector current (ΔI_C) with respect to change in the transistor gain (β) keeping both I_{CO} and V_{BE} constant.

Fixed-Bias Configuration

The expression for collector current is

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

As $I_{CO} << I_B$, therefore $I_C = \beta I_B$.

For $\beta = \beta_1$,

$$I_{C1} = \beta_1 I_B \tag{4.71}$$

For $\beta = \beta_2$,

$$I_{C2} = \beta_2 I_B \tag{4.72}$$

Subtracting Eq. (4.71) from Eq. (4.72), we get

$$I_{C2} - I_{C1} = (\beta_2 - \beta_1) I_B \tag{4.73}$$

Substituting $(I_{C2} - I_{C1})$ as ΔI_C and $(\beta_2 - \beta_1)$ as $\Delta\beta$ in Eq. (4.73), we get

$$\Delta I_C = \Delta\beta I_B \tag{4.74}$$

Equation (4.74) can be rewritten as

$$\frac{\Delta I_C}{\Delta\beta} = I_B = \frac{I_{C1}}{\beta_1} \tag{4.75}$$

Therefore, the value of stability factor S_β for the fixed-bias circuit is given by

$$S_\beta = \frac{I_{C1}}{\beta_1} \tag{4.76}$$

Emitter-Bias Configuration

In the emitter-bias configuration the base current (I_B) is given by

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_E}{R_B + R_E} \tag{4.77}$$

As we know, the expression for collector current (I_C) is given by

$$I_C = \beta I_B + (\beta+1) I_{CO} \tag{4.78}$$

Substituting this value of I_B given by Eq. (4.77) in Eq. (4.78), we get

$$I_C = \frac{\beta(V_{CC} - V_{BE} - I_C R_E)}{R_B + R_E} + (\beta+1) I_{CO} \tag{4.79}$$

Rearranging the terms in Eq. (4.79), we get

$$I_C(R_B + R_E + \beta R_E) = \beta V_{CC} - \beta V_{BE} + (\beta+1)(R_B + R_E) I_{CO} \tag{4.80}$$

As $V_{BE} << V_{CC}$ and $I_{CO} << I_C$, Eq. (4.80) can be approximated as

$$I_C(R_B + R_E + \beta R_E) = \beta V_{CC} \tag{4.81}$$

For $\beta = \beta_1$, Eq. (4.81) can be written as

$$I_{C1}(R_B + R_E + \beta_1 R_E) = \beta_1 V_{CC} \tag{4.82}$$

For $\beta = \beta_2$, Eq. (4.81) can be written as

$$I_{C2}(R_B + R_E + \beta_2 R_E) = \beta_2 V_{CC} \tag{4.83}$$

Subtracting Eq. (4.82) from Eq. (4.83), we get

$$(I_{C2} - I_{C1})(R_B + R_E) + I_{C2}\beta_2 R_E - I_{C1}\beta_1 R_E = (\beta_2 - \beta_1) V_{CC} \tag{4.84}$$

Substituting $(I_{C2} - I_{C1})$ as ΔI_C and $(\beta_2 - \beta_1)$ as $\Delta\beta$ in Eq. (4.84), we get

$$\Delta I_C(R_B + R_E) + I_{C2}\beta_2 R_E - I_{C1}\beta_1 R_E = \Delta\beta V_{CC} \tag{4.85}$$

Adding and subtracting $I_{C1}\beta_2 R_E$ in Eq. (4.85) and then solving we get

$$\Delta I_C(R_B + R_E) + \Delta I_C \beta_2 R_E + I_{C1}\Delta\beta R_E = \Delta\beta V_{CC} \tag{4.86}$$

Rearranging the terms in Eq. (4.86) we get

$$\Delta I_C(R_B + R_E + \beta_2 R_E) = \Delta\beta(V_{CC} - I_{C1} R_E) \tag{4.87}$$

Rearranging the terms in Eq. (4.82) we get

$$V_{CC} = \frac{I_{C1}(R_B + R_E + \beta_1 R_E)}{\beta_1} \tag{4.88}$$

Substituting this value of V_{CC} in Eq. (4.87), we get

$$\Delta I_C(R_B + R_E + \beta_2 R_E) = \Delta\beta\left[\frac{I_{C1}(R_B + R_E + \beta_1 R_E)}{\beta_1} - I_{C1} R_E\right]$$

Therefore,

$$\frac{\Delta I_C}{\Delta\beta} = \frac{I_{C1}(R_B + R_E)}{\beta_1(R_B + R_E + \beta_2 R_E)}$$

$$\frac{\Delta I_C}{\Delta\beta} = \frac{I_{C1}(1 + R_B/R_E)}{\beta_1(1 + \beta_2 + R_B/R_E)}$$

Table 4.1 | Important parameters of different biasing configurations

	I_{CQ}	V_{CEQ}	$S_{I_{CO}}$	$S_{V_{BE}}$	S_β
Fixed bias	$\beta\left(\frac{V_{CC}-V_{BE}}{R_B}\right)$	$V_{CC}-I_{CQ}R_C$	$\beta+1$	$\frac{-\beta}{R_B}$	$\frac{I_{C1}}{\beta_1}$
Emitter bias	$\beta\left(\frac{V_{CC}-V_{BE}}{R_B+(\beta+1)R_E}\right)$	$V_{CC}-I_{CQ}(R_C+R_E)$	$\frac{(\beta+1)(1+R_B/R_E)}{1+\beta+R_B/R_E}$	$\frac{-\beta/R_E}{R_B/R_E+(\beta+1)}$	$\frac{I_{C1}(1+R_B/R_E)}{\beta_1(1+\beta_2+R_B/R_E)}$
Voltage-divider bias	$\beta\left(\frac{V_{TH}-V_{BE}}{R_{TH}+(\beta+1)R_E}\right)$	$V_{CC}-I_{CQ}(R_C+R_E)$	$\frac{(\beta+1)(1+R_{TH}/R_E)}{1+\beta+R_{TH}/R_E}$	$\frac{-\beta/R_E}{R_{TH}/R_E+(\beta+1)}$	$\frac{I_{C1}(1+R_{TH}/R_E)}{\beta_1(1+\beta_2+R_{TH}/R_E)}$
Collector-to-base bias	$\beta\left(\frac{V_{CC}-V_{BE}}{R_B+(\beta+1)R_C}\right)$	$V_{CC}-I_{CQ}R_C$	$\frac{(\beta+1)(1+R_B/R_C)}{1+\beta+R_B/R_C}$	$\frac{-\beta/R_C}{R_B/R_C+(\beta+1)}$	$\frac{I_{C1}(1+R_B/R_C)}{\beta_1(1+\beta_2+R_B/R_C)}$

The value of stability factor (S_β) for the emitter-bias configuration is given by

$$S_\beta = \frac{I_{C1}(1+R_B/R_E)}{\beta_1(1+\beta_2+R_B/R_E)} \tag{4.89}$$

Voltage-Divider Bias with Emitter-Bias Configuration

In the case of voltage-divider-bias configuration, the expression for S_β is similar to that of emitter-bias configuration with the base resistor (R_B) being replaced by Thevenin's equivalent resistance (R_{TH}):

$$S_\beta = \frac{I_{C1}(1+R_{TH}/R_E)}{\beta_1(1+\beta_2+R_{TH}/R_E)} \tag{4.90}$$

Collector-to-Base-Bias Configuration

In the case of collector-to-base-bias configuration, the expression for S_β is similar to that of emitter-bias configuration with the resistance R_E being replaced by R_C:

$$S_\beta = \frac{I_{C1}(1+R_B/R_C)}{\beta_1(1+\beta_2+R_B/R_C)} \tag{4.91}$$

Table 4.1 summarizes the values of quiescent collector current (I_{CQ}), quiescent collector-to-emitter voltage (V_{CEQ}) and stability factors $S_{I_{CO}}$, $S_{V_{BE}}$ and S_β for the various transistor-biasing configurations.

EXAMPLE 4.10 | *Determine the stability factors $S_{I_{CO}}$ $S_{V_{BE}}$ and S_β for each of the following bias arrangements. Also determine the total change in collector current when the temperature changes from +25°C to +175°C. The various transistor parameters at different temperatures are listed in Table 4.2.*

(a) Fixed-bias circuit ($R_B = 300\ k\Omega$, $I_C = 2\ mA$, $\beta = 50$).

(b) Emitter-bias circuit ($R_B = 300\ k\Omega$, $R_E = 2\ k\Omega$, $I_C = 2\ mA$, $\beta = 50$).

(c) Voltage-divider-bias circuit ($R_{B1} = 50\ k\Omega$, $R_{B2} = 10\ k\Omega$, $R_E = 2\ k\Omega$, $I_C = 2\ mA$, $\beta = 50$).

Table 4.2 | Example 4.10.

T(°C)	I_{CO} (nA)	β	V_{BE} (V)
−65	2×10^{-4}	25	0.85
25	0.2	50	0.7
100	25	80	0.5
175	3×10^{3}	125	0.32

Solution

(a) ***Fixed-bias circuit***

1. $S_{I_{CO}} = \beta + 1$. Therefore, $S_{I_{CO}} = 51$.
2. $S_{\beta} = \dfrac{I_{C1}}{\beta_1}$

   where I_{C1} and β_1 are the values of collector current and transistor gain at 25°C, $I_{C1} = 2$ mA and $\beta_1 = 50$.
3. Therefore, $S_{\beta} = 2 \times 10^{-3}/50 = 4 \times 10^{-5}$.
4. $S_{V_{BE}} = -\beta/R_B$. Therefore, $S_{V_{BE}} = -50/(300 \times 10^3) = -16.6 \times 10^{-5}$.
5. Total change in the collector current ΔI_C is

$$\Delta I_C = S_{I_{CO}} \Delta I_{CO} + S_{\beta} \Delta\beta + S_{V_{BE}} \Delta V_{BE}$$

6. $\Delta I_{CO} = (3 \times 10^3 - 0.2)$ nA $\cong 3 \times 10^3$ nA $= 3$ μA.
7. $\Delta\beta = 125 - 50 = 75$.
8. $\Delta V_{BE} = 0.32 - 0.7 = -0.38$.
9. $\Delta I_C = [51 \times 3 \times 10^{-6} + 4 \times 10^{-5} \times 75 + (-16.6 \times 10^{-5})(-0.38)]$ A
   $= (153 + 3000 + 63.08)$ μA $= 3.22$ mA

(b) ***Emitter-bias circuit***

10. $S_{I_{CO}} = \dfrac{(1+\beta)(1+R_B/R_E)}{1+\beta+R_B/R_E}$

$$S_{I_{CO}} = (51)[1+\{(300 \times 10^3)/(2 \times 10^3)\}]/[1+50+\{(300 \times 10^3)/(2 \times 10^3)\}]$$
$$= 51 \times 151/201 = 38.31$$

11. $S_{\beta} = \dfrac{I_{C1}(1+R_B/R_E)}{\beta_1(1+\beta_2+R_B/R_E)}$

    where I_{C1} and β_1 are the values of collector current and transistor gain at 25°C. $I_{C1} = 2$ mA and $\beta_1 = 50$. β_2 is the transistor gain at 175°C with $\beta_2 = 125$.
12. Therefore, $S_{\beta} = (2 \times 10^{-3})[1 + \{(300 \times 10^3)/(2 \times 10^3)\}]/[50(1 + 125 + \{(300 \times 10^3)/(2 \times 10^3)\}] = (302 \times 10^{-3})/(50 \times 276) = 2.19 \times 10^{-5}$.
13. $S_{V_{BE}} = \dfrac{-\beta/R_E}{R_B/R_E + (\beta+1)}$

$$S_{V_{BE}} = \{-50/(2 \times 10^3)\}/[\{(300 \times 10^3)/(2 \times 10^3)\} + 51]$$
$$= -25 \times 10^{-3}/201 = -0.1243 \times 10^{-3} = -12.43 \times 10^{-5}$$

14. Total change in the collector current ΔI_C is

$$\Delta I_C = S_{I_{CO}} \Delta I_{CO} + S_\beta \Delta\beta + S_{V_{BE}} \Delta V_{BE}$$

15. $\Delta I_C = [38.31 \times 3 \times 10^{-6} + 2.19 \times 10^{-5} \times 75 + (-12.43 \times 10^{-5})(-0.38)]$A
$= 1.8$ mA

(c) ***Voltage-divider bias with emitter-bias circuit***

16. $R_{TH} = \dfrac{R_{B1} \times R_{B2}}{R_{B1} + R_{B2}}$

$R_{TH} = (50 \times 10^3 \times 10 \times 10^3)/(50 \times 10^3 + 10 \times 10^3) = 500/60 = 8.3$ kΩ

$$S_{I_{CO}} = \frac{(1+\beta)(1+R_{TH}/R_E)}{1+\beta+R_{TH}/R_E}$$

17. $S_{I_{CO}} = [(51)\{1 + (8.3 \times 10^3)/(2 \times 10^3)\}]/\{1 + 50 + (8.3 \times 10^3)/(2 \times 10^3)\}$
$= 51 \times 5.15/55.15 = 4.76$

18. $S_\beta = \dfrac{I_{C1}(1+R_{TH}/R_E)}{\beta_1(1+\beta_2+R_{TH}/R_E)}$

where I_{C1} and β_1 are the values of collector current and transistor gain at 25°C. $I_{C1} = 2$ mA and $\beta_1 = 50$. β_2 is the transistor gain at 175°C, that is $\beta_2 = 125$.

Therefore,

$$S_\beta = [(2 \times 10^{-3})\{1 + (8.3 \times 10^3)/(2 \times 10^3)\}]/$$
$$(50[1 + 125 + \{(8.3 \times 10^3)/(2 \times 10^3)\}])$$
$$= 10.3 \times 10^{-3}/6507.5 = 1.58 \times 10^{-6}$$

19. $S_{V_{BE}} = \dfrac{-\beta/R_E}{R_{TH}/R_E + (\beta+1)}$

$S_{V_{BE}} = \{-50/(2 \times 10^3)\}/[\{(8.3 \times 10^3)/(2 \times 10^3)\} + 50 + 1]$
$= -25 \times 10^{-3}/55.15 = 0.453 \times 10^{-3} = -45.3 \times 10^{-5}$

20. Total change in the collector current ΔI_C is

$\Delta I_C = S_{I_{CO}} \Delta I_{CO} + S_\beta \Delta\beta + S_{V_{BE}} \Delta V_{BE}$

$\Delta I_C = [4.76 \times 3 \times 10^{-6} + 1.58 \times 10^{-6} \times 75 + (-45.3 \times 10^{-5})(-0.38)]$ A
$= 0.305$ mA

Answer: Fixed-bias circuit: $S_{I_{CO}} = 51$, $S_{V_{BE}} = -16.6 \times 10^{-5}$, $S_\beta = 4 \times 10^{-5}$, $\Delta I_C = 3.22$ mA.

Emitter-bias circuit: $S_{I_{CO}} = 38.31$, $S_\beta = 2.19 \times 10^{-5}$, $S_{V_{BE}} = -12.43 \times 10^{-5}$, $\Delta I_C = 1.8$ mA.

Voltage-divider bias with emitter-bias circuit: $S_{I_{CO}} = 4.76$, $S_\beta = 1.58 \times 10^{-6}$, $S_{V_{BE}} = -45.3 \times 10^{-5}$, $\Delta I_C = 0.305$ mA.

EXAMPLE 4.11

Design an emitter-bias circuit with the following specifications:

(a) change in collector current due to change in leakage current for a temperature range of 25°C to 100°C to be less than or equal to 1 μA;

(b) change in collector current due to change in transistor gain β for a temperature range of 25°C to 100°C to be less than or equal to 400 μA;

(c) change in collector current due to change in base–emitter voltage (V_{BE}) for a temperature range of 25°C to 100°C to be less than or equal to 50 μA;

(d) the quiescent collector-to-emitter voltage is 4 V.

Given that:

$$\text{At } 25^\circ C\ I_{CO} = 0.1\ nA,\ \beta = 50,\ V_{BE} = 0.7;$$
$$\text{at } 100^\circ C\ I_{CO} = 25.1\ nA,\ \beta = 70,\ V_{BE} = 0.4.$$

Solution

1. The desired value of the stability factor $S_{I_{CO}} \le 1 \times 10^{-6}/(25.1 - 0.1) \times 10^{-9} \le 40$. Therefore, the maximum value of $S_{I_{CO}}$ is 40.
2. For an emitter-bias circuit,
$$S_{I_{CO}} = \frac{(1+\beta)(1+R_B/R_E)}{1+\beta+R_B/R_E}$$
3. Substituting $\beta = 50$ in the above expression we get
$$40 = [51 \times (1 + R_B/R_E)]/(51 + R_B/R_E)$$
Therefore, $40\ (51 + R_B/R_E) = [51 \times (1 + R_B/R_E)]$. Therefore, $R_B/R_E = 180.8$.
4. The desired value of the stability factor
$$S_{V_{BE}} \le 50 \times 10^{-6}/(-0.3) \le -16.6 \times 10^{-5}$$
5. The maximum value of $S_{V_{BE}}$ is -16.6×10^{-5}.
6. For an emitter-bias circuit,
$$S_{V_{BE}} = \frac{-\beta / R_E}{R_B/R_E + (\beta+1)}$$
7. Substituing $\beta = 50$ in the above equation, we get
$$-16.6 \times 10^{-5} = (-50/R_E)/(R_B/R_E + 51)$$
8. Therefore, $-16.6 \times 10^{-5}\ (R_B/R_E + 51) = -50/R_E$. That is $R_B/R_E + 51 = 3 \times 10^5/R_E$.
9. Substituting $R_B/R_E = 180.8$ in the above equation, we get
$$R_E = (3 \times 10^5)/231.8 = 1.294\ k\Omega$$
10. The value of $R_B = 180.8 \times 1.294\ k\Omega = 234\ k\Omega$.
11. The desired value of the stability factor $S_\beta \le (400 \times 10^{-6})/(20) \le 2 \times 10^{-5}$.
12. For an emitter-bias circuit,
$$S_\beta = \frac{I_{C1}(1+R_B/R_E)}{\beta_1(1+\beta_2+R_B/R_E)}$$
13. Substituting the value of β_1 as 50 and β_2 as 70 in the above expression, we get
$$2 \times 10^{-5} = I_{C1} \times 181.8/50(71 + 180.8)$$

14. $I_{C1} = 2 \times 10^{-5} \times 50 \times 251.8/181.8 = 1.38$ mA.
15. For the emitter-bias circuit the collector current (I_C) is given by

$$I_C = \frac{\beta(V_{CC} - V_{BE})}{R_B + (\beta+1)R_E}$$

Therefore,

$$1.38 \times 10^{-3} = 50(V_{CC} - 0.7)/(234 \times 10^3 + 51 \times 1.294 \times 10^3)$$

$$V_{CC} = 8.98 \text{ V} \cong 9 \text{ V}$$

16. Applying Kirchhoff's voltage law to the collector–emitter loop, we get

$$9 - I_C R_C - V_{CE} - I_E R_E = 0$$

$$9 - 1.38 \times 10^{-3} \times R_C - 4 - 1.38 \times 10^{-3} \times 1.294 \times 10^3 = 0$$

17. Therefore, $R_C = 2.3$ kΩ.
18. Figure 4.40 shows the design.

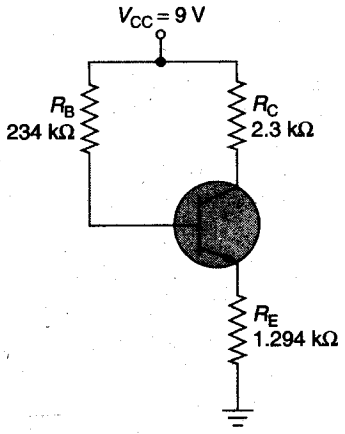


Figure 4.40 | Example 4.11.

4.6 Bias Compensation

The biasing techniques discussed so far offer stability to the operating point (I_{CQ}, V_{CEQ}) by virtue of negative feedback. Although, negative feedback improves stability but it also reduces the gain of the circuit. In applications where the reduction in gain is intolerable, compensation techniques are used to reduce the drift in the operating point.

Compensation techniques make use of temperature-sensitive devices such as diodes, thermistors, transistors, sensitors, etc. to compensate for the changes in the operating point caused due to changes in temperature. In the following sub-sections, we will discuss few of the commonly used compensation circuits.

Diode Compensation for Base–Emitter Voltage (V_{BE})

Figure 4.41 shows a circuit using diode for compensation against variations in base–emitter voltage (V_{BE}) due to change in temperature. The diode is made of the same material as the transistor so that there is same variation

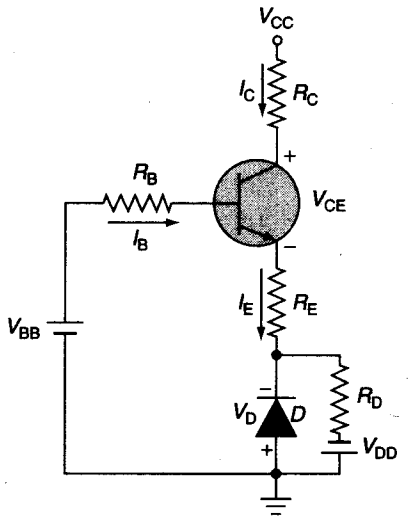


Figure 4.41 | Diode compensation for base–emitter voltage (V_{BE}).

in the transistor's base–emitter voltage (V_{BE}) and diode's forward voltage (V_D) due to temperature. If we examine the circuit, we will see that the circuit is basically an emitter-bias circuit with an additional diode circuitry in the emitter leg. The diode is kept in forward-bias mode through voltage (V_{DD}) and resistance (R_D).

Applying Kirchhoff's voltage law to the base–emitter loop, we get

$$V_{BB} - I_B R_B - V_{BE} - I_E R_E + V_D = 0$$

Substituting $I_E = (\beta + 1) I_B$ in the above equation and solving for base current (I_B), we get

$$I_B = \frac{V_{BB} - (V_{BE} - V_D)}{R_B + (\beta + 1) R_E} \tag{4.92}$$

Collector current (I_C) is related to the base current by the expression

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

Substituting the value of I_B in the expression for collector current, we get

$$I_C = \frac{\beta[V_{BB} - (V_{BE} - V_D)]}{R_B + (\beta + 1) R_E} + (\beta + 1) I_{CO} \tag{4.93}$$

As is clear from Eq. (4.93), the change in the base–emitter voltage (V_{BE}) of the transistor due to the change in temperature will be nullified by a similar change in the forward voltage (V_D) of the diode. In other words, the diode's forward voltage (V_D) tracks the changes in the base–emitter voltage (V_{BE}) of the transistor and compensates for its changes.

Diode Compensation for Leakage Current (I_{CO})

To compensate for the variation in the leakage current (I_{CO}), a diode is placed across the base–emitter terminals of the transistor as shown in Figure 4.42. The diode is reverse-biased and hence the reverse saturation current (I_D) flows through it. The diode is chosen to be of the same material as the transistor, so that the reverse saturation current of the diode increases with temperature at the same rate as the leakage current of the transistor.

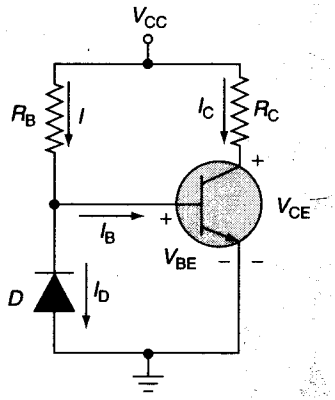


Figure 4.42 | Diode compensation for leakage current (I_{CO}).

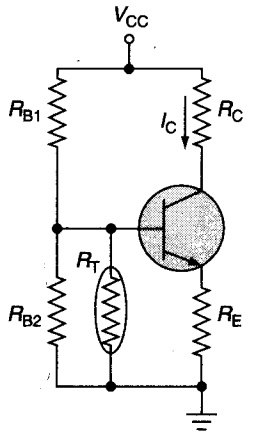


Figure 4.43 | Thermistor compensation.

The base current (I_B) in Figure 4.42 is equal to

$$I_B = I - I_D$$

Substituting this value of base current (I_B) in the expression for collector current (I_C), we get

$$I_C = \beta(I - I_D) + (\beta + 1)I_{CO}$$

As β and $(\beta + 1)$ are nearly equal, the expression for I_C can be written as

$$I_C = \beta I - \beta I_D + \beta I_{CO}$$

Rearranging the terms we get

$$I_C = \beta I - \beta(I_D - I_{CO}) \tag{4.94}$$

The diode reverse current (I_D) tracks the transistor leakage current (I_{CO}) over the desired temperature range.

Thermistor Compensation

Figure 4.43 shows a thermistor-based compensation circuit. The thermistor having negative temperature coefficient of resistance is placed in parallel with resistor R_{B2}. Values of the resistances are so chosen as to establish the desired value of collector current (I_C) at the normal operating temperature. As the temperature increases, the value of the thermistor resistance decreases. This reduces the forward bias and hence the base and collector currents of the transistor. When the temperature decreases, the thermistor resistance increases which results in an increase in the value of base–emitter voltage. This in turn increases the base and the collector currents. Therefore, the thermistor compensates for the change in collector current due to change in temperature.

4.7 Thermal Runaway

The power dissipation capability of a transistor depends upon its physical size, its construction and its mounting arrangement in the system. The maximum power rating is limited by the temperature that the collector-to-base junction can withstand and the ambient temperature. As the ambient temperature increases, the power rating of the transistor decreases. This is referred to as power derating. The power dissipation capability of transistors vary from few to several hundreds of milliwatts in the case of small signal transistors to

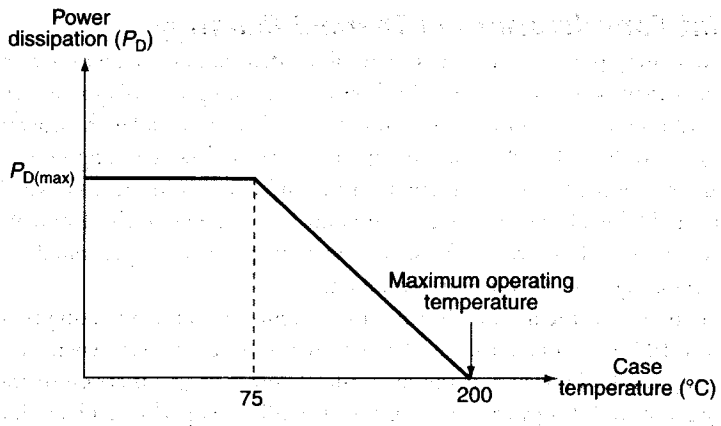


Figure 4.44 | Typical power derating curve of a transistor.

around 250 W in the case of power transistors. As mentioned in Chapter 3, the maximum permissible temperature that the collector-to-base junction of a transistor can handle is in the range of 150°C to 225°C for silicon transistors and 60°C to 100°C for germanium transistors. Figure 4.44 shows the typical power derating curve of a silicon transistor with change in transistor case temperature. It may be mentioned here that in the case of small signal transistors, the case temperature is slightly larger than the ambient temperature and the case and the ambient temperatures are generally considered to be equal. However, in the case of power transistors, case temperature may exceed the ambient temperature by a large amount.

If the transistor circuit is not designed properly, it may lead to the phenomenon of *thermal runway*. When the transistor is in operation it dissipates power and its junction temperature rises, which in turn causes the collector current to increase. This may lead to more power dissipation and further increase in temperature and subsequently a further increase in collector current. If this cycle continues, it may result in permanently damaging the transistor. This phenomenon is referred to as thermal runaway. Proper design of the transistor circuit and selection of a suitable operating point is necessary to prevent the phenomenon of thermal runaway.

The steady-state temperature rise at the transistor collector junction is given by

$$T_J - T_A = \Theta P_D \tag{4.95}$$

where T_J is the transistor junction temperature; T_A the ambient temperature; P_D the power dissipated in the transistor; Θ the thermal resistance (°C/W). *Thermal resistance* is defined as the ratio of the rise in transistor junction temperature to the amount of power dissipated. The value of thermal resistance depends upon the transistor size, the size of heat sink used and other cooling methods used such as forced-air cooling, etc.:

$$\Theta = \frac{T_J - T_A}{P_D} = \frac{dT_J}{dP_D} \tag{4.96}$$

The inverse of the thermal resistance gives the temperature rate at which the power is dissipated under steady-state conditions:

$$\frac{dP_D}{dT_J} = \frac{1}{\Theta} \tag{4.97}$$

The condition for thermal stability is that the rate at which heat is generated at the collector junction should not exceed the rate at which it can be dissipated under steady-state conditions.

Operating-Point Considerations in Thermal Runaway

The position of the operating point of the transistor amplifier determines whether the transistor is inherently stable against thermal runaway or not. Figure 4.45 shows the various power dissipation curves of a transistor and a typical DC load line for an emitter-bias configuration. Let us consider the operating point Q_1. The DC load line is tangent to the 200 mW power dissipation curve at the operating point. An increase in the collector current due to internal heating or increase in the ambient temperature causes the operating point to shift upwards on the DC load line. The operating point is now between the 100 mW and the 200 mW power dissipation curves. Therefore, with increase in temperature the power generated decreases. Hence, the circuit is inherently stable against variations in temperature.

For the operating point Q_2, the increase in collector current causes the operating point to shift upwards and move towards the 100 mW curve. This results in reduction in the power generated. Hence, the circuit is inherently thermally stable. However, if the operating point is at Q_3, increase in the collector current causes the operating point to shift upwards towards the 200 mW curve. This results in increase in the power generated. Hence, the circuit is not inherently thermally stable and may lead to thermal runaway. Such a circuit needs to be checked for thermal stability.

The thumb rule to decide whether the operating point is in the safe region of operation is that for operating point with collector-to-emitter voltage (V_{CEQ}) less than $V_{CC}/2$ the circuit is thermally stable as increase in collector current results in reduced power generation. In the case of operating points having V_{CEQ} greater than $V_{CC}/2$, the circuit is not inherently thermally stable. In such cases, it is necessary to check the thermal characteristics of the transistor and the circuit design to ensure thermal stability.

For such circuits to be thermally stable they should satisfy the following condition:

$$[V_{CC} - 2I_C(R_E + R_C)](S_{I_{co}})(0.07I_{CO}) < 1/\Theta \tag{4.98}$$

where V_{CC} is the supply voltage; I_C the collector current; R_E the emitter resistor; R_C the collector resistor; $S_{I_{co}}$ the stability factor; I_{CO} the leakage current; Θ the thermal resistance of the transistor. This equation is valid for the emitter-bias circuit of Figure 4.11 redrawn again in Figure 4.46 for the convenience of the readers. In the case of fixed-bias circuit, Eq. (4.98) is valid with $R_E = 0$.

The mathematical treatment to the theoretical concepts described for thermal runaway phenomenon is given in the subsequent paragraphs.

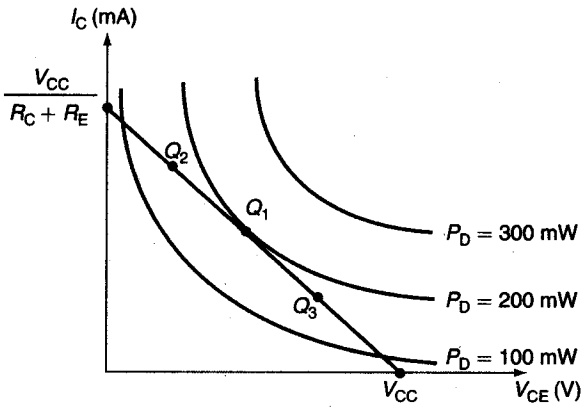


Figure 4.45 | Operating-point considerations against thermal runaway.

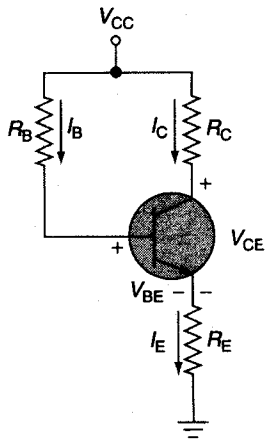


Figure 4.46 | Emitter-bias circuit.

For the emitter-bias circuit in Figure 4.46, the power produced in the transistor is given by

$$P_G = I_C V_{CB} \cong I_C V_{CE} \tag{4.99}$$

where P_G is the power produced in the transistor; I_C the collector current; V_{CB} the collector–base voltage; V_{CE} the collector–emitter voltage. Now $V_{CE} = V_{CB} + V_{BE}$. Assuming V_{BE} to be negligible as compared to V_{CB} and V_{CE}, we have $V_{CE} \cong V_{CB}$.

The collector–emitter voltage (V_{CE}) in emitter-bias circuit is expressed by

$$V_{CE} = V_{CC} - I_E R_E - I_C R_C \tag{4.100}$$

As $I_E \cong I_C$, Eq. (4.100) can be approximated as

$$V_{CE} \cong V_{CC} - I_C (R_E + R_C) \tag{4.101}$$

Substituting the value of V_{CE} given in Eq. (4.101) in Eq. (4.99), we get

$$P_G = I_C V_{CC} - I_C^2 (R_E + R_C) \tag{4.102}$$

Differentiating Eq. (4.102) with respect to collector current (I_C), we get

$$\frac{dP_G}{dI_C} = V_{CC} - 2I_C (R_E + R_C) \tag{4.103}$$

The required condition for thermal stability is that the rate at which heat is produced at the collector junction should not exceed the rate at which it can be dissipated by the transistor under steady-state conditions. Rate of heat generated at the collector junction is given by differentiating the power generated (P_G) with respect to the junction temperature. Therefore, for thermal stability the following equation should be satisfied:

$$\frac{dP_G}{dT_J} < \frac{dP_D}{dT_J} \tag{4.104}$$

From Eq. (4.97) we know that

$$\frac{dP_D}{dT_J} = \frac{1}{\Theta}$$

Therefore, the requirement for thermal stability is given by

$$\frac{dP_G}{dT_J} < \frac{1}{\Theta} \tag{4.105}$$

Multiplying and dividing the LHS of Eq. (4.105) by dI_C we get

$$\frac{dP_G}{dT_J} \times \frac{dI_C}{dI_C} < \frac{1}{\Theta}$$

Rearranging the terms in the LHS of the equation we get

$$\frac{dP_G}{dI_C} \times \frac{dI_C}{dT_J} < \frac{1}{\Theta} \tag{4.106}$$

where dI_C/dT_J is the rate at which the collector current changes with junction temperature. Since $1/\Theta$ and dI_C/dT_J are both positive, therefore the above equation is always true when dP_G/dI_C is negative. From Eq. (4.103) we know that

$$\frac{dP_G}{dI_C} = V_{CC} - 2I_C(R_E + R_C)$$

Therefore to ensure thermal stability, the following equation should be satisfied:

$$V_{CC} - 2I_C(R_E + R_C) < 0 \tag{4.107}$$

Rearranging the terms in Eq. (4.107), we get

$$I_C > \frac{V_{CC}}{2(R_E + R_C)} \tag{4.108}$$

We know that in emitter-bias configuration

$$V_{CE} = V_{CC} - I_C(R_E + R_C)$$

Substituting the value of I_C in the equation we infer that when the collector–emitter voltage (V_{CE}) is less that half the supply voltage ($V_{CE} < V_{CC}/2$), then the circuit is thermally stable under all conditions. For $V_{CE} > V_{CC}/2$, the term dP_G/dI_C is positive and therefore the circuit design should be done such that Eq. (4.106) is satisfied.

The collector current (I_C) changes with the change in temperature as the leakage current (I_{CO}), the base–emitter voltage (V_{BE}) and the transistor gain (β) change with temperature. The rate of change of collector current with junction temperature is given by

$$\frac{dI_C}{dT_J} = S_{I_{CO}} \frac{dI_{CO}}{dT_J} + S_{V_{BE}} \frac{dV_{BE}}{dT_J} + S_\beta \frac{d\beta}{dT_J} \tag{4.109}$$

However in most cases the effect of leakage current (I_{CO}) is far more than that of transistor gain (β) and the base–emitter voltage (V_{BE}). Therefore,

$$\frac{dI_C}{dT_J} \cong S_{I_{CO}} \frac{dI_{CO}}{dT_J} \tag{4.110}$$

Substituting the value of dI_C/dT_J in Eq. (4.106), we get

$$\left(\frac{dP_G}{dI_C}\right)(S_{I_{CO}})\left(\frac{dI_{CO}}{dT_J}\right) < \frac{1}{\Theta} \tag{4.111}$$

$dI_{CO}/dT_J = 0.07I_{CO}$ as the reverse saturation current increases at a rate of approximately 7%/°C. Substituting the value of dP_G/dI_C [Eq. (4.103)] and the value of dI_{CO}/dT_J in Eq. (4.111), we get

$$[V_{CC} - 2I_C(R_C + R_E)](S_{I_{co}})(0.07I_{CO}) < \frac{1}{\Theta} \tag{4.112}$$

From Eq. (4.112) we can infer that for small signal transistors the problem of thermal runaway is not so critical as these transistors have small value of collector current (I_C) and small value of stability factor ($S_{I_{CO}}$). However, power transistors have higher value of collector current (I_C) and stability factor and hence thermal management is a major problem in the case of power transistors. One of the thermal management techniques to increase the power handling capability of transistors is to make use of heat sinks. Design of heat sinks is discussed in detail in the chapter on power transistors.

EXAMPLE 4.12

Figure 4.47 shows the circuit of a transformer-coupled power amplifier. Determine whether the circuit is thermally stable. If not, determine the junction to ambient thermal resistance (Θ_{J-A}) required so that the transistor operates safely at an ambient temperature of 25°C. It is given that the transistor gain β at 25°C is 100, the leakage current I_{CO} at 25°C is 1 mA, the maximum junction operating temperature is 100°C, the base–emitter voltage of the transistor is 0.7 V.

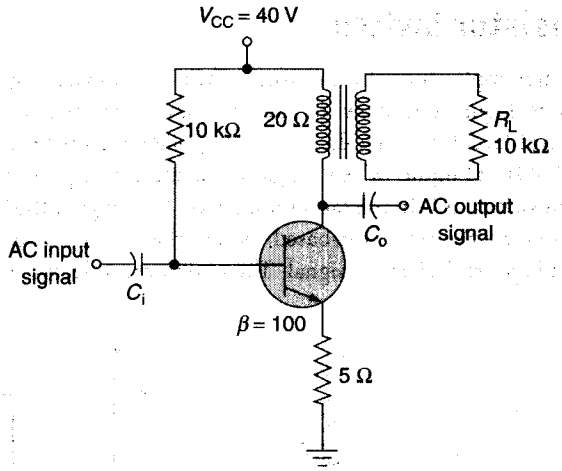


Figure 4.47 | Example 4.12.

Solution

1. $I_C = \beta I_B + (\beta + 1)I_{CO}$
   $= 100 \times I_B + 101 \times 1 \times 10^{-3}$
   $= 100I_B + 0.101$

2. Applying Kirchhoff's voltage law to the emitter–base loop, we get
   $$40 - 10 \times 10^3 \times I_B - 0.7 - 5 \times I_E = 0$$
   Subtituting $I_E = (\beta + 1)I_B = 101I_B$, we get $I_B = 3.74$ mA, $I_C = 374$ mA and $I_E \cong I_C = 374$ mA.

3. Applying Kirchhoff's voltage law to the collector–emitter loop, we get

$$40 - 20 \times I_C - V_{CE} - 5 \times I_E = 0$$

$$V_{CE} = 40 - 20 \times 374 \times 10^{-3} - 5 \times 374 \times 10^{-3} = 30.65$$

4. As $V_{CE} > V_{CC}/2$, therefore the circuit is not inherently thermally stable.
5. The quiescent power generated is given by

$$V_{CEQ} \times I_{CQ} = 30.65 \times 374 \times 10^{-3} = 11.46 \text{ W}$$

6. The power dissipation capability is given by $(T_J - T_A)/\Theta_{J\text{-}A}$.
7. For thermal stability $(100 - 25)/(\Theta_{J\text{-}A}) \geq 11.46$. Therefore, $(\Theta_{J\text{-}A}) \leq 6.54°C/W$.

Infact, transformer-coupled transistor amplifiers are very much susceptible to thermal runaway as they have very small DC resistance in the collector circuit (transformer primary and the emitter resistor).

Answer: The circuit is not thermally stable. The maximum value of thermal resistance is 6.54°C/W.

4.8 Transistor Switch

Another major application of transistors is their use as switching devices in computers and other control applications. Figure 4.48 shows the use of a transistor as an inverting switch, that is the transistor output is at logic-HIGH level for a logic-LOW input applied at its base terminal and the output is at logic-LOW level for a logic-HIGH input. When a logic-LOW input is applied, the transistor is in the cut-off region and acts as an open switch. It is in the saturation region for a logic-HIGH input and acts as a closed switch.

While designing the transistor-based switch, the designer should ensure that the transistor is heavily saturated for a logic-HIGH input signal. The saturation collector current ($I_{C(sat)}$) is given by the equation

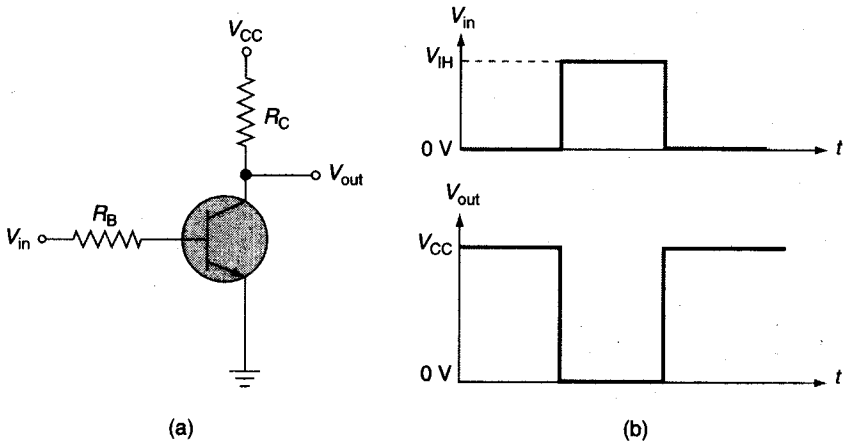


Figure 4.48 | Transistor switch.

$$I_{C(sat)} = \frac{V_{CC}}{R_C} \tag{4.113}$$

The level of base current (I_B) in the active region just before the saturation region can be approximated by

$$I_{B(sat)} = \frac{I_{C(sat)}}{\beta}$$

The base current ($I_{B(max)}$) is generally kept to be 20–25% more than the value of $I_{B(sat)}$ so as to ensure that the transistor is in deep saturation. Therefore, the ratio of the collector current to the base current when the logic-HIGH input is applied is less than the transistor current gain (β). The minimum value of input voltage (V_{IH}) required to drive the transistor into deep saturation so that it acts as a closed switch is given by

$$V_{IH} = I_{B(max)}R_B + V_{BE} \tag{4.114}$$

The resistance between the emitter and the collector terminals when the transistor is in saturation is given by

$$R_{sat} = \frac{V_{CE(sat)}}{I_{C(sat)}} \tag{4.115}$$

The resistance offered by the transistor switch when in saturation is equal to R_{sat}. The value of R_{sat} is in the range of few ohms to few tens of ohms.

For input voltage equal to zero, the collector current (I_C) is equal to the leakage current (I_{CO}) which is negligible. Therefore the collector voltage is at the logic-HIGH level and the value of collector–emitter resistance is very high in the range of several hundreds of kilo-ohms to few mega-ohms. The circuit thus acts as an open circuit.

Transistor Switching Delays

Figure 4.49 shows the response of a transistor switch when an input pulse is applied to it. When the input voltage is 0 V, the transistor is in the cut-off region. It is in the saturation region when the input voltage is at

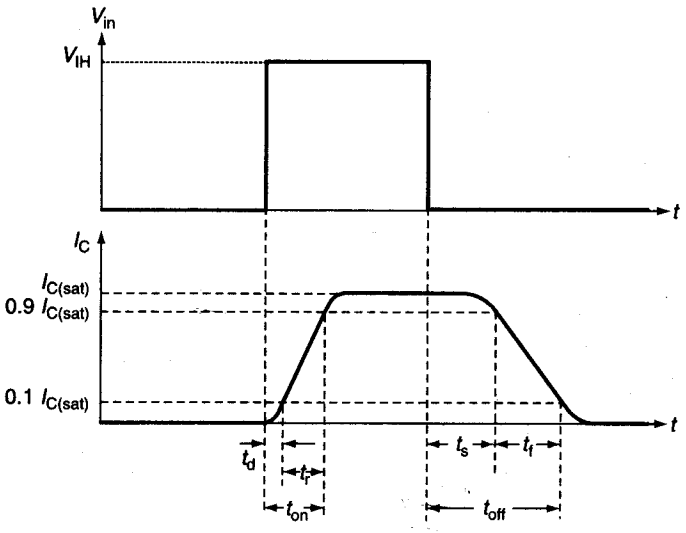


Figure 4.49 | Transistor switching times.

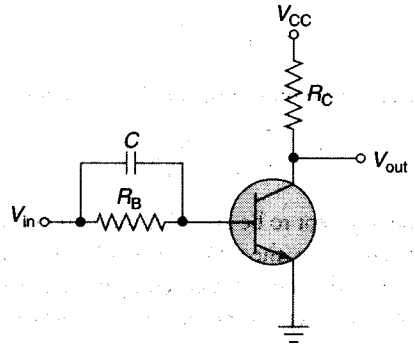


Figure 4.50 | Fast switching transistor circuit.

the voltage level V_{IH}. When the input voltage changes from 0 V to V_{IH}, the transistor does not immediately respond to the input signal and there is a time delay before the collector current reaches the saturation value. The time delay between the time the input pulse is applied to the time the collector current rises to 10% of the final value is called the *delay time* (t_d).

The time required for the collector current to rise from 10% to 90% of the final value is called the *rise time* (t_r). The total time ($t_d + t_r$) is known as the *turn-ON time* (t_{on}) of the transistor. Delay time (t_d) is contributed by three factors: First, the time required to charge the emitter-junction capacitance so that the transistor is brought from the cut-off to the active region; second, the time required to move the carriers from the base junction to the collector junction; third, the time required by the collector current to rise to 10% of its final value. Rise time (t_r) is due to the time taken by the collector current to traverse the active region.

When the input signal returns to 0 V, again there is a delay between the transition of the input waveform and the time when the collector current reduces to zero. The time interval between the input pulse transition to the time when the collector current drops to 90% of its value at saturation is called the *storage time* (t_s). Storage time delay is because the transistor in saturation has a saturation charge of excess minority carriers stored in the base region and the transistor cannot respond until this excess charge has been removed. *Fall time* (t_f) is the time required by the collector current to fall from 90% to 10% of the saturation level. Fall time is caused due to the time required by the collector current to traverse the active region. *Turn-OFF time* (t_{off}) is defined as the sum of the storage time (t_s) and the fall time (t_f).

When the transistor is used in fast switching applications, a capacitor (C) is added across the base resistor (R_B) to reduce the storage time (Figure 4.50). The capacitor will act as a short circuit when switching occurs and an impulse current will flow out of the base at the negative transition of the input pulse.

EXAMPLE 4.13 | *An input pulse is applied to the transistor switch shown in Figure 4.51. What is the minimum input voltage required to make the LED glow? Also, find out the minimum input voltage required to put the transistor in saturation. It is given that the minimum current required by the LED to glow is 10 mA, voltage drop across the LED is 1.5 V, base–emitter voltage of the transistor is 0.7 V, collector–emitter voltage of the transistor in saturation is 0.5 V.*

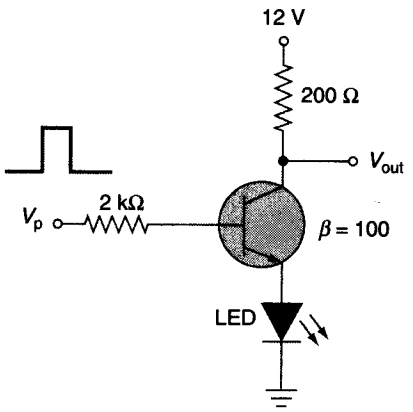


Figure 4.51 | Example 4.13.

Solution

1. The minimum current required to make the LED glow is 10 mA and the voltage drop across the LED is 1.5 V.
2. Therefore, the collector current required to make the LED glow is 10 mA. As β of the transistor is 100, therefore the base current (I_B) required is 100 μA.
3. Applying Kirchhoff's voltage law to the base–emitter loop, we get
$$V_P - 2 \times 10^3 \times 100 \times 10^{-6} - 0.7 - 1.5 = 0$$
$$V_P = 2.4 \text{ V}$$
4. Therefore, the minimum voltage required to make the LED glow is 2.4 V.
5. When the transistor is in saturation, $V_{CE(sat)} = 0.5$ V. Therefore, applying Kirchhoff's voltage law to the collector–emitter loop, we get
$$12 - 200 \times I_{C(sat)} - 0.5 - 1.5 = 0$$
$$I_{C(sat)} = 50 \text{ mA}$$
6. The value of $I_{B(sat)}$ corresponding to this value of $I_{C(sat)}$ is 500 μA.
7. The value of $I_{B(max)}$ is kept 1.25 times this value of $I_{B(sat)}$ to ensure that the transistor is in saturation. Therefore, $I_{B(max)} = 625$ μA.
8. Applying Kirchhoff's voltage law to the base–emitter loop and solving for V_P, we get
$$V_P = 0.7 + 1.5 + 2 \times 10^3 \times 625 \times 10^{-6} = 3.45 \text{ V}$$
9. The input voltage required to put the transistor into saturation is 3.45 V.

Answer: The minimum voltage required to make the LED glow is 2.4 V. The input voltage required to put the transistor into saturation is 3.45 V.

EXAMPLE 4.14

A simple logic circuit is configured as shown in Figure 4.52(a). The input voltages V_3 and V_4 applied to the circuit are plotted in Figure 4.52(b). Draw the output waveform across resistor R_5. Assume $V_{CE(sat)} = 0$.

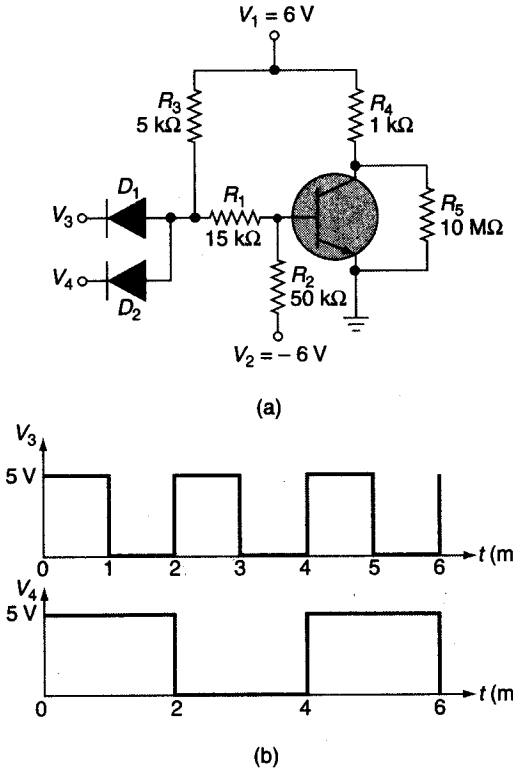


Figure 4.52 | Example 4.14.

Solution

1. When either or both of the inputs are low, then one or both of the diodes D_1 and D_2 are conducting. Therefore, the voltage at the R_1–R_3 node is 0.7 V. The transistor is not-conducting and the collector–emitter voltage is 6 V.
2. When both inputs are high, then both the diodes D_1 and D_2 are not conducting and the base voltage is determined by voltages V_1 and V_2 and resistors R_1, R_2 and R_3.
3. The base voltage can be determined using superposition theorem.
4. Assuming $V_1 = 0$ [Figure 4.53(a)], the voltage due to V_2 at base terminal is

$$V_{B2} = -(5+15) \times \frac{6}{5+15+50} = -20 \times \frac{6}{70} = -1.7 \text{ V}$$

5. Assuming $V_2 = 0$ [Figure 4.53(b)], the voltage due to V_1 at base terminal

$$V_{B1} = 50 \times \frac{6}{5+15+50} = 50 \times \frac{6}{70} = 4.3 \text{ V}$$

6. Base voltage = 4.3 V − 1.7 V = 2.6 V.
7. This base voltage drives the transistor into saturation. As is given, the value of collector–emitter voltage when the transistor is in saturation is zero. The waveform across R_5 is the same as that of the collector–emitter voltage of the transistor (Figure 4.54).

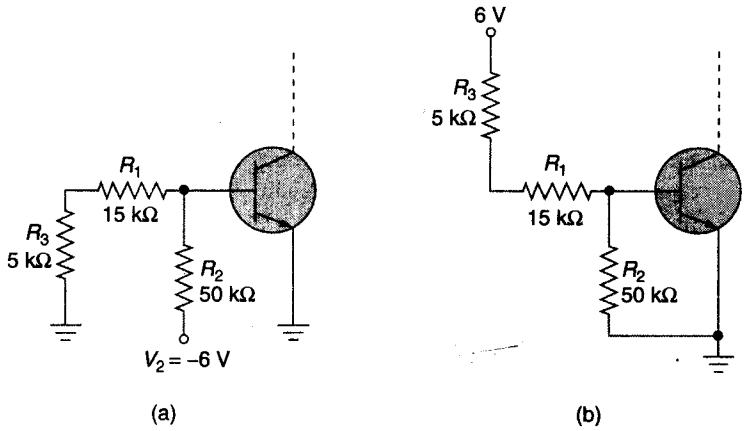


Figure 4.53 | Solution to Example 4.14.

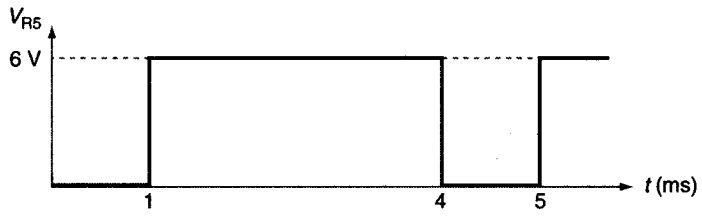


Figure 4.54 | Solution to Example 4.14.

KEY TERMS

Collector-to-base-bias configuration
Compensation techniques
Emitter-bias configuration
Fixed-bias configuration
Operating point
Stability factor
Voltage-divider bias with emitter-bias configuration

OBJECTIVE-TYPE EXERCISES

Multiple-Choice Questions

1. In the fixed-bias circuit if the base resistor is shorted then
   a. the transistor may get damaged.
   b. the base voltage will be zero.
   c. the collector voltage will be equal to the supply voltage.
   d. the collector current is zero.
2. The common-collector bias and emitter-bias are examples of
   a. voltage-series feedback.
   b. voltage-series feedback and voltage-shunt feedback, respectively.
   c. voltage-series feedback and current-series feedback, respectively.
   d. current-series feedback and current-shunt feedback, respectively.
3. Which of the following conditions ensures that the transistor does not undergo thermal runaway?
   a. $V_{CE} = V_{CC}/2$

b. $V_{CE} < V_{CC}/2$
c. $V_{CE} < V_{CC}$
d. $V_{CE} > V_{CC}/2$

4. The delay time of the transistor switch is due to
   a. time required to charge the emitter-junction capacitance so that the transistor is brought from the cut-off to the active region.
   b. time required to move the carriers from the base to the collector junction.
   c. time required by the collector current to rise to 10% of its final value.
   d. all the above.
5. In a transistor switch the relationship between collector current (I_C) and the base current (I_B) is
   a. $I_C = I_B$
   b. $I_C = \beta I_B$
   c. $I_C > \beta I_B$
   d. $I_C < \beta I_B$
6. In the fixed-bias configuration if the supply voltage changes, the slope of the load line
   a. increases.
   b. decreases.
   c. remains the same.
   d. may increase or decrease.
7. The biasing configuration that offers least stability is
   a. fixed-bias configuration.
   b. collector-to-base-bias configuration.
   c. voltage-divider-bias configuration.
   d. none of the above.
8. The input resistance in case of emitter-bias circuit is equal to
   a. $(\beta + 1)R_B + R_E$
   b. $\beta R_B + (\beta + 1)R_E$
   c. $R_B + (\beta + 1)R_E$
   d. $R_B + R_E$
9. A transistor switch operates in
   a. either saturation or cut-off region.
   b. active region.
   c. either active or cut-off region.
   d. either saturation or active region.
10. In the emitter-bias circuit the voltage across the emitter resistance is equal to
    a. voltage between the emitter and collector.
    b. voltage between the emitter and ground.
    c. voltage between the collector and base.
    d. voltage between the collector and ground.

Match the Following

Choose the correct one from among the alternatives A, B, C, D after matching an item from Group 1 with the most appropriate item in Group 2.

Group 1	Group 2
1: Emitter bias	P: operating point
2: Transistor switch	Q: negative feedback
3: Thermal runaway	R: positive feedback
4: Active region	S: forward-biased base–emitter junction and reverse-biased collector–emitter junction
	T: cut-off and saturation
	U: zero V_{BE} and V_{CE}

(A) 1-Q, 2-T, 3-P, 4-S
(B) 1-R, 2-T, 3-R, 4-Q
(C) 1-U, 2-P, 3-S, 4-R
(D) 1-T, 2-Q, 3-P, 4-S

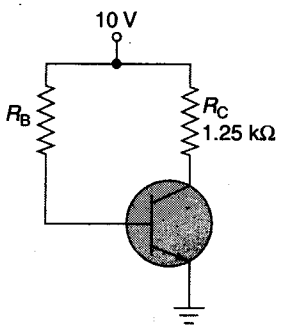
REVIEW QUESTIONS

1. With the help of common-emitter amplifier configuration, explain the criteria for selection of a suitable operating point and the factors affecting its stability.

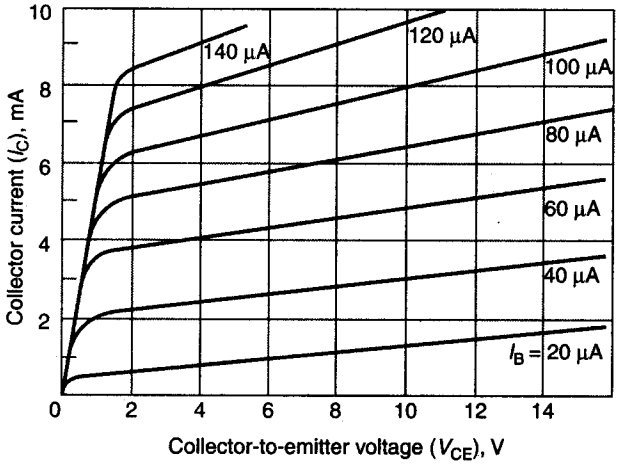
2. Derive the mathematical expression to prove that the operating point in voltage-divider-bias configuration is independent of transistor gain β.
3. Draw the circuit for collector-to-base-bias configuration and derive the value of stability factors $S_{I_{CO}}$, S_β and $S_{V_{BE}}$ for the circuit.
4. Explain the operation of a transistor switch. What are the steps to be followed to design a transistor switch?
5. Derive the expressions for the stability factor ($S_{I_{CO}}$) for
   a. fixed-bias configuration;
   b. self-bias configuration;
   c. voltage-divider-bias configuration.
6. What is the drawback of emitter-bias configuration? How is the drawback removed in the voltage-divider bias with emitter-bias configuration?
7. Draw the following circuits using PNP transistors and derive the expressions for the operating point for each of the cases:
   a. fixed-bias configuration;
   b. voltage-divider-bias configuration;
   c. collector-to-base-bias configuration.
8. When is a transistor amplifier circuit inherently stable against thermal runaway? Support the answer with relevant mathematical expressions.
9. Give reasons for the following:
   a. Why is bias compensation required?
   b. Power transistors are more prone to thermal runaway as compared to small signal transistors?
   c. Why is fixed-bias circuit not commonly used?
   d. Why is the operating point chosen near the center of the active region of the transistor characteristics in a transistor amplifier?
10. Define the following terms
    a. power derating;
    b. thermal resistance of a transistor;
    c. turn-ON time of a transistor switch;
    d. bias compensation.

PROBLEMS

1. Figures 4.55(a) and (b) show a fixed-bias circuit and the output characteristics of the transistor used in the circuit (assume base–emitter voltage of transistor = 0.7 V). Determine:
   a. DC load line;
   b. the value of resistor R_B for base current of 40 μA;
   c. the operating point (I_C, V_{CE});
   d. the value of transistor gain β.



(a)



(b)

Figure 4.55 | Problem 1.

2. Find the operating point of the emitter-bias circuit shown in Figure 4.56. Design a voltage-divider bias with emitter-bias circuit having the same operating point (assume base–emitter voltage of transistor = 0.7 V).

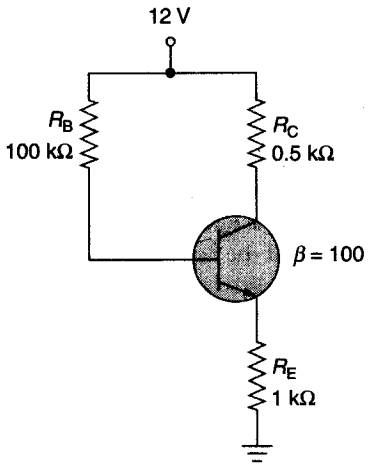


Figure 4.56 | Problem 2.

3. Figure 4.57 shows a circuit using a PNP transistor. Find the value of V_{out}. Assume base–emitter voltage of transistor = 0.7 V.

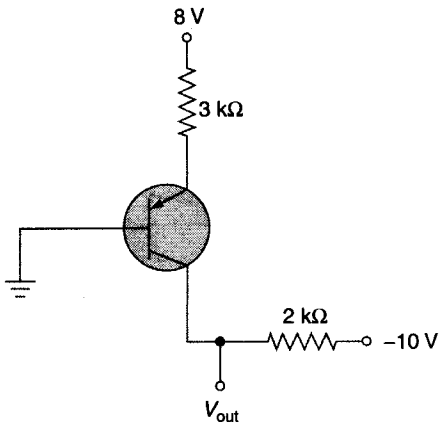


Figure 4.57 | Problem 3.

4. Draw the DC equivalent of the circuit shown in Figure 4.58. Also find the collector voltage of transistors Q_1 and Q_2? Assume $V_{BEQ1} = V_{BEQ2} = 0.7$ V.

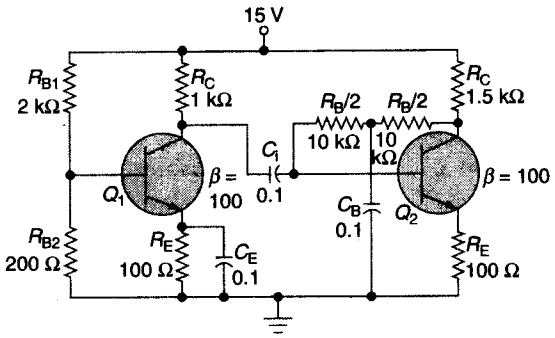


Figure 4.58 | Problem 4.

5. For the network in Figure 4.59, find the value of $S_{I_{CO}}$, $S_{V_{BE}}$ and S_β and the total change in collector current for a temperature change of 25°C to +100°C. It is given that at 25°C: $I_{CO} = 0.2$ nA, $\beta = 50$ and $V_{BE} = 0.7$ V; and at 100°C: $I_{CO} = 25$ nA, $\beta = 80$ and $V_{BE} = 0.5$ V.

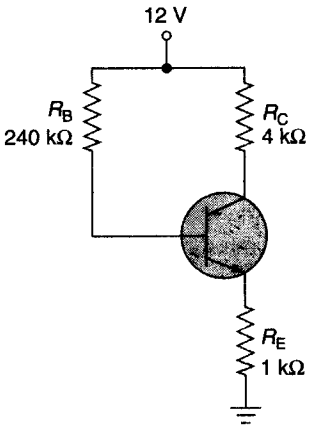


Figure 4.59 | Problem 5.

6. Design an emitter-bias circuit with the following specifications: $I_C = 10$ mA, $V_{CE} = 4$ V, $V_{CC} = 15$ V, $R_C/R_E = 10$. It is given that β is 130 and V_{BE} is 0.7 V.

7. Figure 4.60 shows the transistor-based inverter circuit with the desired output waveform for the given input waveform. Find the value of V_{CC}, R_C and R_B given that $\beta = 80$, $I_{C(sat)} = 10$ mA, the output voltage V_{out} when the transistor is off is 12 V, $V_{BE} = 0.7$ V.

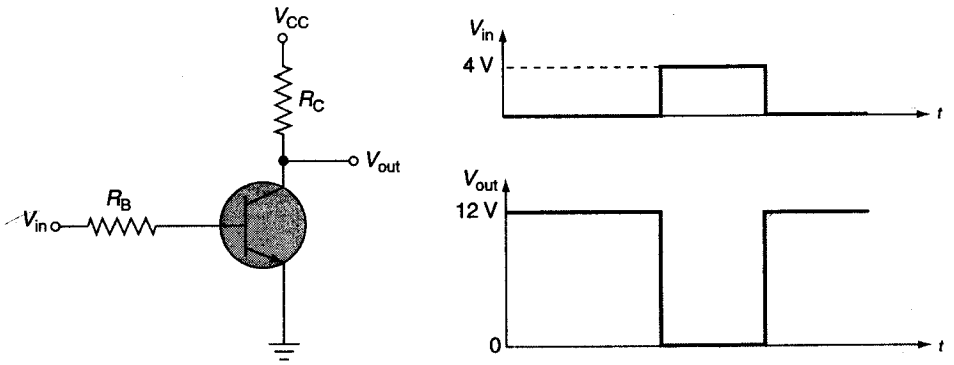


Figure 4.60 | Problem 7.

8. (a) Refer to Figure 4.61. Calculate the value of R_B if $V_{CE} = 5$ V.

(b) For $R_B = 50$ kΩ, determine the value of V_{CEQ}. Also, determine whether the circuit is inherently thermally stable. It is given that the base–emitter voltage of the transistor is 0.7 V.

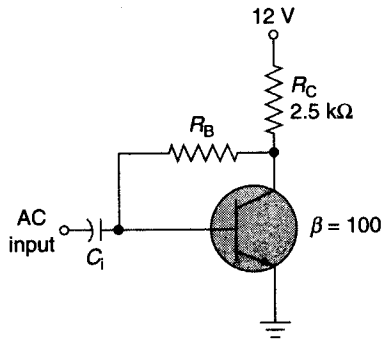


Figure 4.61 | Problem 8.

ANSWERS

Multiple-Choice Questions

1. (a)	**3.** (b)	**5.** (d)	**7.** (a)	**9.** (a)
2. (c)	**4.** (d)	**6.** (c)	**8.** (c)	**10.** (b)

Match the Following

Answer (A).

Problems

1. (a) Figure 4.62; (b) 232.5 kΩ; (c) (2.7 mA, 6.6 V); (d) 67.5

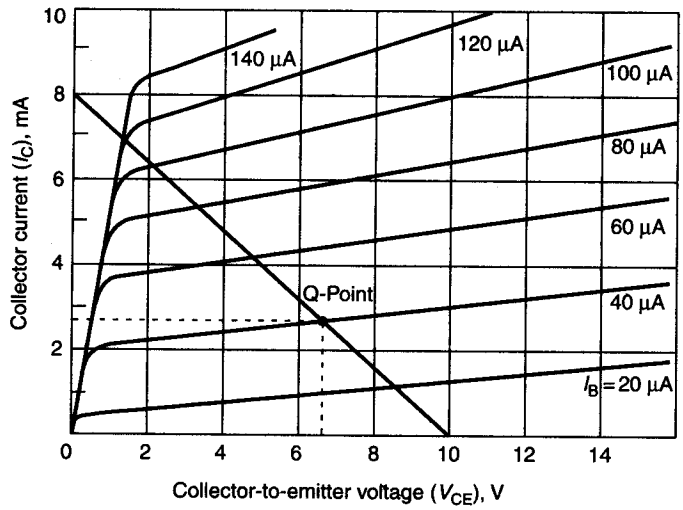


Figure 4.62 | Solution to part (a) of Problem 1.

2. (5.62 mA, 3.57 V); Figure 4.63

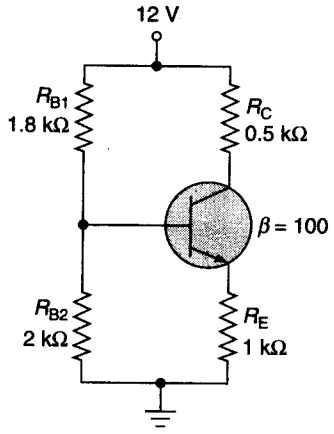


Figure 4.63 | Solution to Problem 2.

3. −5.14 V

4. Figure 4.64; $V_{CQ1} = 8.58$ V; $V_{CQ2} = 3.07$ V

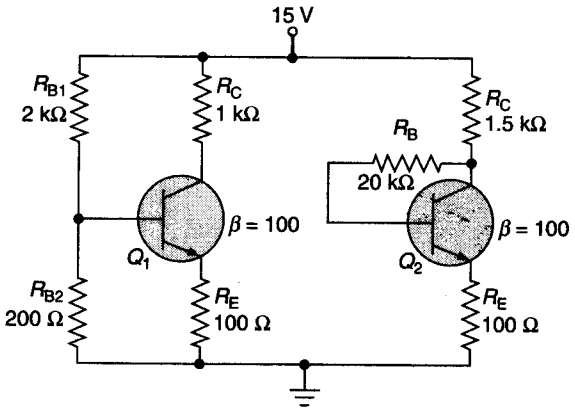


Figure 4.64 | Solution to Problem 4.

5. $S_{I_{CO}} = 42.24$, $S_{V_{BE}} = -0.17 \times 10^{-3}$, $S_\beta = 2.92 \times 10^{-5}$, $\Delta I_C = 0.911$ mA

6.

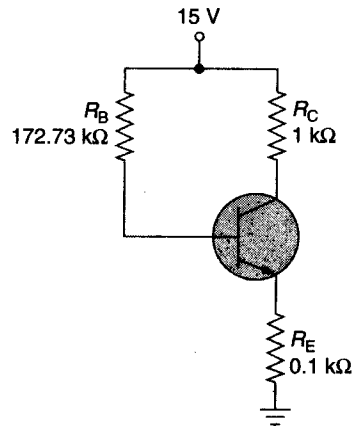


Figure 4.65 | Solution to Problem 6.

7. $V_{CC} = 12$ V, $R_C = 1.2$ kΩ, $R_B = 21.12$ kΩ

8. (a) 153.57 kΩ, (b) 2.6 V; the circuit is thermally stable